

# A Half-Bridge Buffer Circuit with Clamped Energy Feedback

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Configuring half-bridge circuits with CRC or RC circuits at both ends of the bus, RC circuits at both ends of the device, and in conjunction with reduced loop inductance is a typical solution to address half-bridge switching oscillations and voltage overshoots, and to optimize electromagnetic interference (EMI) characteristics. However, this scheme still has the problems of poor damping effect, high degree of overvoltage, and high turn-on loss. In this paper, we remove the switch-by-switch RC circuit to reduce extra losses, actively increase the inductance of the feeder circuit to achieve zero current turn-on, and design a DC(VS)-RC absorption topology with energy return circuits at both ends of the bus. The designed topology absorbs the overvoltage energy stored in the inductor of the switching converter and feeds it back to the bus to reduce the overvoltage and improve efficiency. Experimental studies and comprehensive comparative studies verify the effectiveness of the proposed scheme. The experimental results show that DC(VS)-RC with increasing loop inductance has good overvoltage and oscillation suppression performance and can significantly reduce the switching losses.

**KEYWORDS**

Overvoltage and oscillation, *SiC MOSFET*, snubber circuit, switching losses optimization

# 1 | INTRODUCTION

The half-bridge converter topology uses two power switching devices connected in a totem pole format to provide a square-wave signal with the midpoint as the output. Half-bridge topologies have been widely used in many structures such as PWM motor control, DC-AC inverters with electronic ballasts, etc. [1, 2, 3, 4, 5]. Since the voltage stress on the transistors is about twice that of the push-pull, single-ended excitation, or interleaved forward topologies, the half-bridge topology has been developed for high voltage environments [6, 7]. However, the switching devices of half-bridge circuits always have overvoltage and oscillation problems due to the parasitic inductance of the switching devices. In recent years, with the development of semiconductor industry, wide-bandgap (WBG) devices have been more widely used. For example, SiC MOSFETs are used in half-bridge circuits, and faster switching speeds are achieved by using WBG devices. The power density of the half-bridge circuit is improved [8, 9, 10]. However, the high switching frequency of WBG devices increases the sensitivity of devices to loop parasitic parameters, which will lead to more serious high voltage and current stress[11], ringing during switching[12] instability, and electromagnetic interference (EMI) noise[13, 14].

In order to solve these problems, a passive damping buffer circuit is configured for the half-bridge circuit. They are the passive resistor-capacitor (RC) damping circuit equipped device by device and the passive capacitance resistance capacitance (CRC) absorption circuit at both ends of the bus. Moreover, the printed circuit board (PCB) of the half-bridge circuit was designed to minimize the feed-loop inductance. The design structure of the passive damping buffer circuit is simple, but the energy absorbed in the buffer capacitor will be dissipated in the resistor. Although the energy loss in a single switching process reaches  $\mu\text{J}$  level, the heat generated in the converter application cannot be ignored, especially in the high-voltage, high-current and high-frequency fields. And when designing RC and CRC circuits, there is a contradiction between overvoltage absorption and oscillation damping, which leads to limited suppression effect [15, 16, 17, 18, 19]. In addition, the small loop inductance makes the  $di/dt$  become larger and the current rise phase advance when the half-bridge is opened, which increases the turn-on loss of the half-bridge circuit. When the half-bridge topology with SiC MOSFETs is operated, the turn-on loss will be four times the turn-off loss [20]. In the practical application of half-bridge circuits, decreasing loop inductance increases full switching losses [21], and even if the switching loss is sacrificed, overvoltage and vibration damping may not be as effective as required. A certain amount of stray inductance is inevitable and the voltage stress problem still exists when the switching speed increases [22]. In [23, 24, 25, 26, 27], several passive lossless buffer circuits have been proposed in which the leakage sensing energy of the high-frequency switching devices is transferred to the input power supply. In addition, these circuits allow for soft-switching conditions, as well as zero-voltage switching (ZVS) and zero-current switching (ZCS) of switching devices. However, these circuits have high requirements on the operating point of the converter, which brings a large current stress to the main switching device of the converter, and these passive methods greatly increase the complexity of the circuit. Compared to the passive buffer circuit scheme described above, the active clamp circuit can suppress voltage spikes while maintaining the soft-switching condition of the semiconductor, and it has a higher efficiency compared to dissipation and passive buffers, but the losses of the absorption circuit are large. Therefore, under the premise of ensuring a low circuit complexity and a good damping effect, the current research focus is further reduction of the loss of the buffer circuit to improve circuit efficiency.

To address this issue, this paper designs an overvoltage and oscillation suppression circuit with a dual-capacitor topology, incorporating switch loss optimization and clamping energy feedback functions. First, zero-voltage switching (ZVS) of the half-bridge circuit is achieved by utilizing layout-assisted inductance. The increase in loop inductance reduces the  $di/dt$  in the half-bridge loop, thereby reducing induced noise and switching losses, while ensuring zero-current switching (ZCS) of the switching devices. In addition, this design enables the storage of overvoltage energy, reducing the energy stored in the parasitic inductance of the switching devices. Furthermore, a DC(VS)-RC damping topology is employed to suppress overvoltage oscillations. The dual-capacitor absorption structure allows the use of an LLC resonant converter to provide a boost feedback of the overvoltage energy. By combining these methods, the typical RC circuits used in damping absorption schemes can be eliminated, thus



reducing the losses in individual components. In the designed damping absorption topology, the absorption part employs a DC(VS) design, which decouples overvoltage absorption from damping, greatly reducing the choice of capacitance values in the damping section's RC circuits. This reduction also lessens the constraints on the absorption capacitors, enabling more efficient energy feedback for overvoltage suppression. Through the optimization of switch losses, the removal of individual RC circuits, and the single-feedback approach for overvoltage energy, this design effectively reduces the power losses during the feedback process. The combination of zero-current turn-on for the switches, removal of individual RC circuits, and single-feedback for overvoltage energy ensures both the loss optimization of the half-bridge circuit's buffer stage and the effective suppression of overvoltage oscillations.

The remainder of this paper is organized as follows. In Section 2, the proposed half-bridge damping buffer circuit topology and principle are analyzed. Section 3 theoretically compares DC(VS)-RC with typical schemes. In Section 4, the basic performance of the proposed damped absorption topology is experimentally compared and discussed with that of a typical damped absorption topology. Finally, Section 5 concludes the paper.

## 2 | PROPOSED DAMPED ABSORPTION CIRCUIT FOR HALF BRIDGE CIRCUITS

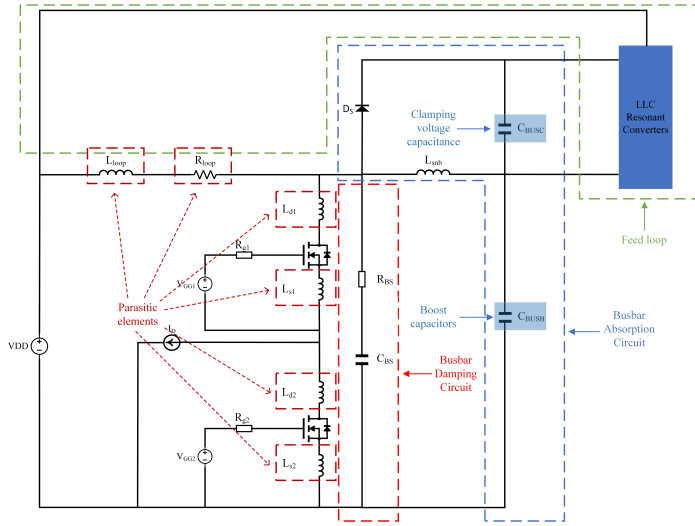
### 2.1 | Circuit Topology

The proposed half-bridge circuit applying SiC MOSFETs to realize a soft turn-on clamped DC(VS)-RC absorption damping topology with energy feedback is shown in Fig. 1. Where  $L_{loop}$  and  $R_{loop}$  represent the parasitic inductance and resistance in the feeder circuit, and  $L_d$  and  $L_s$  represent the parasitic inductance of the drain and source of the two switching devices, respectively. The DC(VS)-RC absorbing damping topology consists of two components. First, a damping circuit consisting of  $R_{BS}$  and  $C_{BS}$  is used to handle the oscillations at both ends of the bus. Secondly, a clamp absorber circuit consisting of  $D_s$ ,  $C_{BUSC}$ ,  $C_{BUSB}$ , and feed loop LLC resonant converter is used to absorb the spike voltage at both ends of the bus and complete the energy feedback. For absorption circuits,  $C_{BUSC}$  can be charged to the bus voltage through  $L_{snb}$  before the start of switching device operation in the half-bridge circuit. The negative terminal of  $C_{BUSC}$  is connected to the positive terminal of  $C_{BUSB}$ , so that  $C_{BUSB}$  realizes the function of pulling up the voltage of  $C_{BUSC}$ . The LLC resonant converter is connected only at the ends of  $C_{BUSC}$  for feeding back the overvoltage portion of the energy to the ends of the bus, and the energy in  $C_{BUSB}$  is not involved in the feedback that reducing the power magnitude at the time of feeding.

### 2.2 | Main working principle

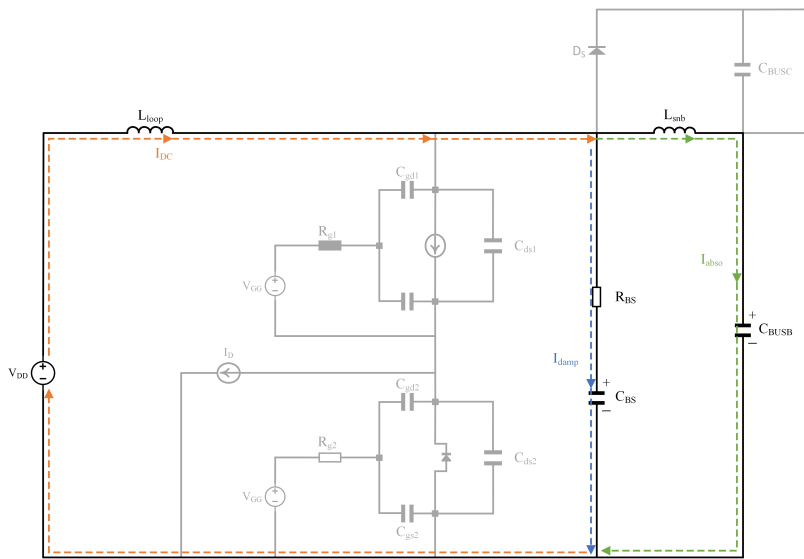
#### 2.2.1 | Preparatory Process

When opened, DC bus voltage increases and the damping circuit partially charges  $C_{BS}$  by forming  $I_{damp}$  through the action of  $R_{BS}$ ; In the absorption circuit section, charging of  $C_{BUSB}$  is accomplished by  $L_{snb}$ , pulls up the potential of  $C_{BUSC}$ . Until the voltage of  $C_{BS}$  and  $C_{BUSB}$  reach the bus voltage, the startup process is complete. One thing to keep in mind during this process is that the values of  $R_{BS}$  and  $L_{snb}$  should be as large as possible, this is to keep them from affecting the circuit afterward. A small  $R_{BS}$  will cause the RC circuit to affect the voltage of the low-side MOSFET during the turn-on phase of the half-bridge circuit when the RC circuit releases the energy of  $C_{BS}$  through the half-bridge circuit; The small  $L_{snb}$  cannot achieve the effect of decoupling the  $C_{BUSB}$  from the half-bridge after the startup process and introduces new influences. At the same time, these values should not be too large to ensure appropriate duration. Due to the design initiative to add the auxiliary inductor in the feeder circuit and the use of SMD SiC MOSFETs,  $L_d$  and  $L_s$  are small enough compared to  $L_{loop}$ , and most of the overvoltage

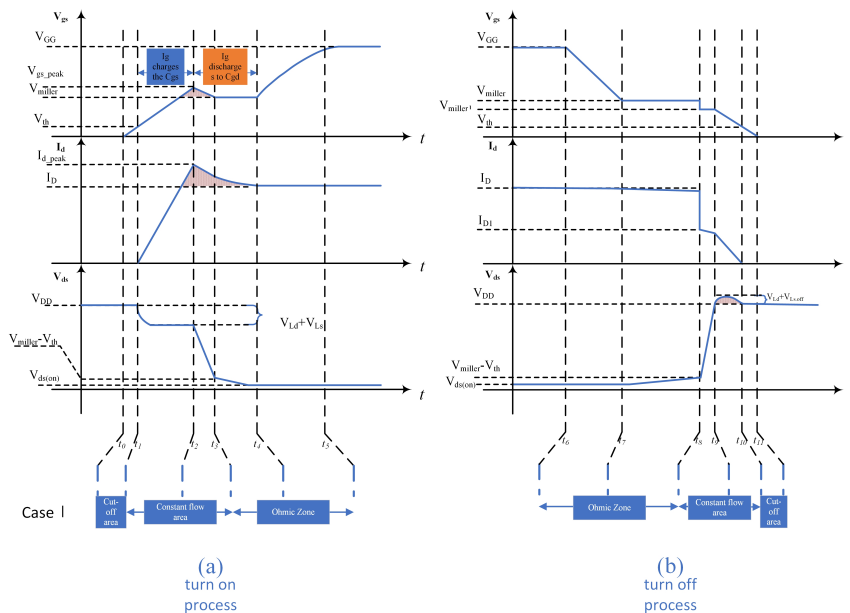


**FIGURE 1** Proposed DC(VS)-RC in a half-bridge configuration

energy is preserved in the  $L_{loop}$  in commutation process, so the parasitic inductance of the drain-source  $L_d$  and  $L_s$  of the device is ignored in analysis. The circuit modes are shown in Fig. 2.



**FIGURE 2** Preparatory process of the proposed DC(VS)-RC



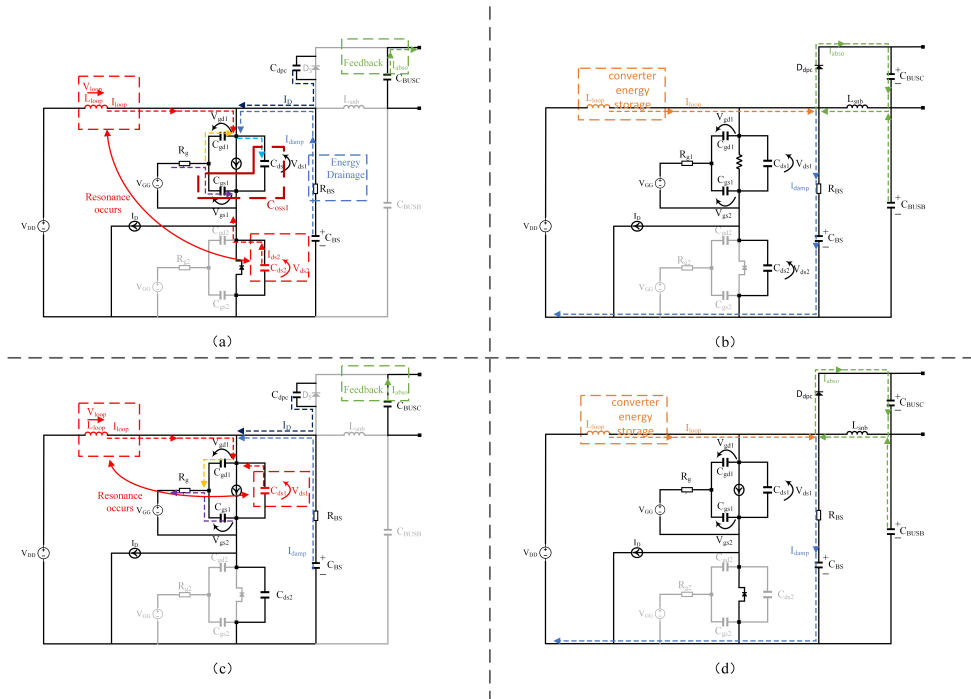
**FIGURE 3** Half-bridge switching high-side SiC MOSFET switching waveforms. (a) Turn-on process. (b) Turn-off process

Fig. 3 shows the waveform of the switching cycle of the high-side MOSFET of the half-bridge circuit, in which overvoltage and oscillation occur at both ends of the bus of the half-bridge circuit during the turn-on phase and the turn-off phase.

### 2.2.2 | Turn-ON Process

Taking the waveform of the half-bridge high-side MOSFET as an example, a current peak occurs during the current rise phase in the stage ( $t_1 - t_2$ ), and this peak is due to the reverse recovery current of the half-bridge low-side SiC MOSFET. In stage ( $t_2 - t_3$ ), the low-side MOSFET of the half-bridge produces voltage peaks, and oscillations are generated by the resonance between the parasitic capacitor  $C_{oss2}$  and the loop inductor  $L_{loop}$  due to the voltage mutation of  $C_{oss2}$ . At this time, the damping absorption circuit of the half-bridge circuit is used to deal with the overvoltage and oscillation generated by the low-side MOSFET of the half-bridge.

In the current rise phase ( $t_1 - t_2$ ) as in Fig. 4(a), the absorption circuit capacitor  $C_{busc}$  completes the energy feedback through the LLC resonant converter at this time. It is worth noting that at this time the capacitance of the RC circuit  $C_{bs}$  through the half-bridge circuit for the energy drain, which will reduce the voltage peak of the lower half-bridge MOSFETs at this time, but this value is very small, and this effect will be ignored in the following analysis. In the turn-on overvoltage phase ( $t_2 - t_3$ ) as shown in Fig. 4(b), the damping absorption circuit starts to work in this phase, and due to the symmetry of the half-bridge circuit, the following analysis takes the DC(VS)-RC absorption damping topology for handling turn-OFF overvoltage as an example.



**FIGURE 4** Switching transients in proposed DC(VS)-RC snubber circuits

### 2.2.3 | Turn-OFF Process

Take the half-bridge high-side MOSFET waveform as an example, the ( $t_8 - t_9$ ) phase is a current drop phase, after which the ( $t_9 - t_{10}$ ) phase generates a voltage peak in the MOSFET at the upper end of the half-bridge. And due to the sudden changes in current, the loop inductance  $L_{loop}$  resonates with the parasitic capacitance  $C_{oss1}$  of the half-bridge high-side MOSFET to generate oscillations, and at this time, the half-bridge circuit damping absorption circuit is used to deal with the overvoltage and oscillations generated by the high-side MOSFET of the half-bridge. For ease of analysis in this section, the diode voltage drop has a negligible effect on the circuit.

a) Current down phase ( $t_8 - t_9$ ): At this stage, the current  $I_d$  starts to decrease and starts to charge  $C_{ds1}$ , and the voltage starts to rise under the action of the MOSFET gate drive circuit on the high side of the half-bridge. The decrease in current leads to an induced voltage across the loop inductor  $L_{loop}$ , causing the loop inductor to resonate with the parasitic capacitance of the half-bridge high-side MOSFET and the parasitic capacitance of the absorption circuit diode. At this stage, the voltage across the absorption circuit has reached  $V_{DD}$  due to the preparatory phase. As a result, the cathode voltage of  $D_s$  is higher than that of the anode, and the diode  $D_s$  is blocked by current. In this time, the damping absorption circuit temporarily does not affect the operation of the half-bridge circuit, and the overvoltage absorption capacitor  $C_{busc}$  completes the energy return.

b) Overvoltage clamping ( $t_9 - t_{10}$ ): At this point, the voltage across the bus exceeds  $V_{DD}$  due to the induced voltage generated by the loop inductance. Due to the action of  $C_{busb}$  the voltage value of  $C_{busc}$  is  $V_{DD}$ , then diode  $D_s$  conducts positively and the damping absorption circuit starts working. The complete isolation of the absorption circuit from the half-bridge loop is realized due to the action of the diode  $D_s$  and the inductor  $L_{snb}$ . The two absorption capacitors  $C_{busb}$  and  $C_{busc}$  have no new effect on the half-bridge circuit, only the parasitic capacitance of the diode has an effect on the half-bridge circuit, but this effect

has a positive effect to be analyzed later.

By analyzing, the energy is preserved in  $L_{loop}$  during the operation of the half-bridge circuit consists of two components which are the overvoltage energy due to the induced currents and the energy available at the ends of the bus itself. where the overvoltage energy is determined by the magnitude of the overvoltage.

According to the law of conservation of energy, the value of the overvoltage in the half-bridge circuit at this point can be approximated as:

$$\frac{1}{2}(L_{loop})I_D^2 = \frac{1}{2}(C_{oss} + C_{dpc})V_{os}^2 \quad (1)$$

$$V_{os} = \sqrt{\frac{L_{loop}}{C_{oss} + C_{dpc}}} I_D \quad (2)$$

Where  $I_d$  is the MOSFET drain current.  $C_{oss}$  is the sum of  $C_{ds}$  and  $C_{gs}$ , the output capacitance of the MOSFET.  $C_{dpc}$  is the parasitic capacitance of diode  $D_s$ , this value can be referenced in the device datasheet.

Where the overvoltage energy stored by the inductor is:

$$E_{loop} = \frac{1}{2}(L_{loop})I_D^2 \quad (3)$$

The absorption capacitance  $C_{busc}$  accomplishes the absorption of the overvoltage energy through  $D_s$ . The absorption circuit absorbs charge at this time can be approximated:

$$Q_{OS} = \sqrt{L_{loop} \cdot C_{busc}} I_D \quad (4)$$

Then the magnitude of the clamp voltage is:

$$V_{busc} = \frac{Q_{OS}}{C_{busc}} = \sqrt{\frac{L_{loop}}{C_{busc}}} I_D \quad (5)$$

The drain-source voltage  $V_{ds1}$  of the high-side MOSFET can be determined as:

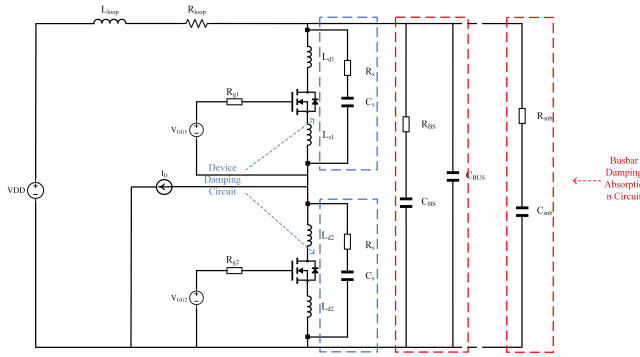
$$V_{ds1} = V_{DD} + V_{CD} + V_{busc} \quad (6)$$

$$I_{Cbusc} = C_D \frac{dv_{CD}}{dt} = C_{busc} \frac{dv_{Cbusc}}{dt} \quad (7)$$

Where  $C_D$  and  $V_{CD}$  are the parasitic capacitance of the absorber circuit diode  $D_s$  and the value of the voltage across it. Since  $C_{busc} \gg C_D$ , we get  $\frac{dv_{CD}}{dt} \gg \frac{dv_{Cbusc}}{dt} \approx 0$ . Thus, a relationship exists:

$$\frac{dv_{ds1}}{dt} = \frac{dv_{CD}}{dt} \quad (8)$$

c) Energy feedback to the dc side ( $t_{10} - t_{11}$ ): At  $t_{10}$ , the commutation time period ends, which means that the turn-off



**FIGURE 5** Typical damped absorption topology

processing of the half-bridge high-side MOSFET is finished.  $V_{ds1}$  drops to  $V_{DD}$ ,  $C_{busc}$  absorbs almost all of the overvoltage energy, the voltage across the absorber circuit is significantly higher than  $V_{DD}$ , and  $D_s$  turns off. The energy is preserved in  $C_{busc}$  begins to be fed back to both ends of the bus through the LLC resonant converter.  $V_{busc}$  falls and the energy feedback current  $I_{abso}$  rises. Until  $t_{11}$ , the voltage on the absorber circuit side is again equal to VDC and the period ends. At this stage, the absorption circuit is composed of two capacitors,  $C_{busb}$  and  $C_{busc}$ , where the role of  $C_{busb}$  is to increase the voltage value of  $C_{busc}$  so that it can complete the absorption of the overvoltage part of the energy and feedback.

d) Damping phase( $t_8 - t_{11}$ ): Since this paper actively increases the inductance value of the feeder circuit and uses switching devices in SMD packages with low parasitic parameters. Almost all of the oscillation and overvoltage energy is stored in the feed-loop inductor. Therefore, the choice was made to remove the RC damping circuits employed in each switch, and the choice was made to employ one RC damping circuit at both ends of the busbar to deal with the oscillations.

### 3 | COMPARISON WITH TYPICAL DAMPED ABSORPTION TOPOLOGY

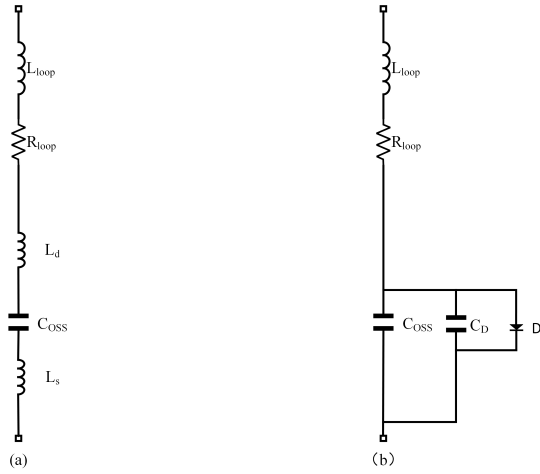
#### 3.1 | Damping absorption effect

For a typical damped absorption topology, the RC circuits at both ends of the device and the RC or CRC circuits at both ends of the bus handle the oscillation of the switching devices, and the overvoltage spikes are handled by the RC and CRC at both ends of the bus, as shown in Fig. 5.

With respect to the oscillation problem, the oscillation of a half-bridge circuit applying a typical damped-absorption topology is mainly due to the resonance of the loop parasitic inductance with the switching device parasitic capacitance. During any switching transient, the potential of the half-bridge AC node changes abruptly between 0 V and  $U_{DC}$ , resulting in resonance between the parasitic elements. The parasitic inductance of the integrated loop of the resonant network is equivalent to  $L_{loop}$ , the parasitic inductance of the drain and source of the device are  $L_d$  and  $L_s$  respectively, the loop resistance  $R_{loop}$  and the output capacitor  $C_{OSS}$  of SiC MOSFET constitute the RLC series resonant circuit, and the equivalent diagram is shown in Fig. 6(a).

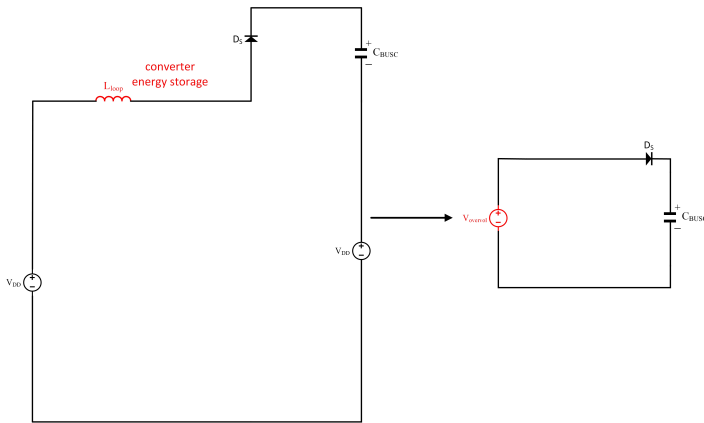
For the half-bridge circuit applying the DC(VS)-RC absorption topology, due to the presence of the diode  $D_s$  in the absorption circuit, the decoupling of the absorption capacitor and the half-bridge circuit is realized. And when the switch device starts to work, the alternating current is generated by the alternating conduction of the upper and lower switch devices, and the equivalent capacitance in the RLC resonant network is the parallel equivalent capacitance of the output capacitor  $C_{OSS}$  of SiC MOSFET and the parasitic capacitor  $C_D$  of diode  $D_s$  because of the characteristic of the capacitor to AC and DC. Since the parasitic capacitance value of the diode is on the order of pf, this equivalent capacitance is greatly reduced, and its equivalent

diagram is shown in Fig. 6(b). Therefore, when choosing the capacitor of the damping circuit, the half-bridge circuit with DC(VS)-RC absorption topology can achieve a better damping effect with a smaller capacitance.



**FIGURE 6** Equivalent diagram of a resonant circuit

For handling voltage spikes, typical solutions rely on the circuits at both ends of the bus to handle overvoltage, but during the process of handling and absorption, the overvoltage energy will be repeatedly lost on the resistor, and the remaining overvoltage energy will be re-discharged through the switching device during the opening of the half-bridge. For the half-bridge circuit with DC(VS)-RC absorption topology, the absorption equivalent diagram is shown in Fig. 7. In this process, due to the existence of auxiliary inductor and  $C_{busb}$ ,  $C_{busb}$  can be regarded as the same voltage source as the bus voltage, and the feeding loop inductor  $L_{loop}$  can be regarded as a voltage source where the overvoltage energy is concentrated. In this case, the absorption process can be simply equivalent to a power supply charging  $C_{busc}$  through diode  $D_s$ , and completing the feedback of bus voltage in the subsequent feedback stage.



**FIGURE 7** Overvoltage absorption equivalent diagram

### 3.2 | Losses Analysis

1) Switching Losses: For the switching loss of the half-bridge circuit, the turn-on and turn-off are discussed separately. For the SiC MOSFET, the turn-on loss is about four times of the turn-off loss due to the reverse recovery problem. In this paper, the turn-on loss of SiC MOSFET is greatly reduced by increasing the power loop inductance. SiC MOSFETs can be made to operate in the loss-optimized region by adjusting the power ring inductance during conduction.

The switching loss of the switching devices is expressed by Equation (9), which is the area of overlap of current and voltage in the switching process.

$$P_{SW} = \int_{t_a}^{t_b} U_{ds} \cdot I_d dt \quad (9)$$

Where  $t_a$  and  $t_b$  represent the start time and end time when the current and voltage begin to overlap, respectively. The DC(VS)-RC absorption topology reduces the voltage spike and convergence time, and reduces the switching loss.

The small loop inductance reduces the turn-OFF overvoltage, but the turn-on loss of SiC MOSFET is still serious, the switching loss is not significantly reduced, and the parasitic inductance in the package of the switching devices also stores a large amount of energy. The heat of the switching devices itself increases, and the difficulty of heat dissipation is increased. The DC(VS)-RC absorption topology actively adds auxiliary inductors to realize the switching of ZCS and greatly optimizes the half-bridge switching loss.

2) Other Losses: Other losses of the DC(VS)-RC absorption topology include loss of the damping part and loss of the absorption parts. The damping part is the RC circuit, and there is the same loss as in the typical scheme. This loss can be estimated by the energy stored in the capacitor, as shown in Equation (10).

$$E_C = \frac{1}{2} C_{snb} U_{DD}^2 \quad (10)$$

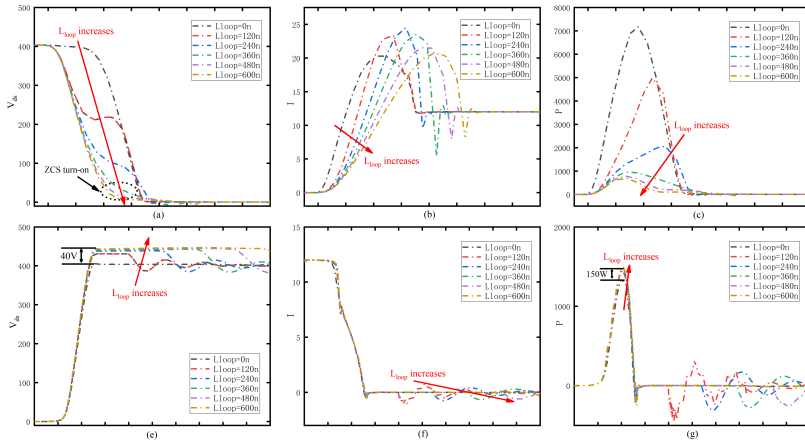
Where  $C_{snb}$  is the capacitor value of the RC circuit and  $U_{DD}$  is the value of voltage at both ends of the capacitor at this time.

The RC circuit charges C through resistance R and discharges C through resistance R. In this cycle, the loss energy generated by the RC circuit is  $2E_C$ . Therefore, the value of the capacitor at the same voltage at the two ends of the capacitor determines the size of this loss. According to the above analysis of the equivalent diagram of the resonant circuit, when the capacitance size of the RC circuit of DC(VS)-RC is designed, only 10 nF can be used to achieve the damping effect, that is, only 1.6  $\mu$ J of energy loss is generated in one cycle.

For the absorption circuit, it consists of only one SiC diode and two capacitors. The charge loss of SiC diodes due to junction capacitor charging and discharging is only a few microjoules, which can be neglected. Losses in the buffer and energy feedback process are also low. Because the feedback energy is only the energy of the overvoltage part and is a conduction loss and has only a short duration, so the loss caused by the DC(VS)-RC absorption topology is negligible compared to the loss of the switching devices.

For a typical damped absorption topology scheme, the RC circuits at both ends of the device and the RC or CRC circuits at both bus ends both introduce new losses to the half-bridge circuit. By analyzing the energy storage size of each part of the capacitor, the loss size of each part of the typical scheme can be approximated at this time. Among them, the RC part will produce corresponding losses on the resistor and switching devices during the charging and discharging process of the capacitor, and the single capacitor part will produce losses on the switching devices during its discharging process, and these losses will cause the temperature of the switching devices to rise. The heat loss caused by the damping absorption circuit at both ends of the device or the bus leads to the aggravation of the heat dissipation problem of the switching devices.





**FIGURE 8** Turn-On and Turn-Off Current/Voltage Transients and Switching Losses in Half-Bridge Circuits with Applied DC(VS)-RC Snubber Circuits with Changing Loop. (a) Turn-ON voltage fall period. (b) Turn-ON current rise period. (c) Turn-off switching losses. (e) Turn-OFF voltage rise period (f) Turn-OFF current fall period. (g) Turn-off switching losses.

### 3.3 | Parameter Selections

By comparing the two schemes, it can be found that the parameter design of DC(VS)-RC absorption topology mainly focuses on the auxiliary inductance  $L_{loop}$  of feeding loop, the value of resistance  $R_{BS}$  and capacitance  $C_{BS}$  of damping circuit, and the value of capacitance  $C_{BUSB}$  and  $C_{BUSC}$  of absorption circuit.

#### 3.3.1 | Power Loop Parasitic Inductance $L_{loop}$ :

According to the analysis in Chapter 2, the selection of  $L_{loop}$  needs to meet two requirements. The first is to ensure that the SiC MOSFET can achieve ZVS soft switching. Secondly,  $L_{loop}$  is required to store as much energy as possible to complete the interaction with the absorption circuit and accomplish the commutation and storage of energy. And RC circuit at both ends of the device is removed to reduce the heat loss of the switching devices. Firstly, the relationship between the current and voltage of the loop inductor  $L_{loop}$  and the half-bridge is obtained through simulation experiments, and its ZVS region is determined, as shown in Fig. 8. Through observation and analysis, when  $L_{loop}$  reaches 600 nH, SiC MOSFET can basically achieve ZVS soft turn-on. Large loop inductance will cause an increase in turn-OFF overvoltage, but according to the design of the clamp absorption circuit in this paper, this overvoltage value can be not worried when selecting the loop auxiliary inductor. As shown in Fig. 8(e), the turn-OFF overvoltage of the half-bridge circuit with DC(VS)-RC absorption topology does not increase significantly with the increase of  $L_{loop}$ . According to the formula of inductive energy storage:

$$E_L = \frac{1}{2} L_{loop} I_d^2 \quad (11)$$

In order to make the feed loop auxiliary inductance have higher energy storage compared with the parasitic inductance of the device itself, the loop auxiliary inductance is chosen to be set to 1.2 uH.

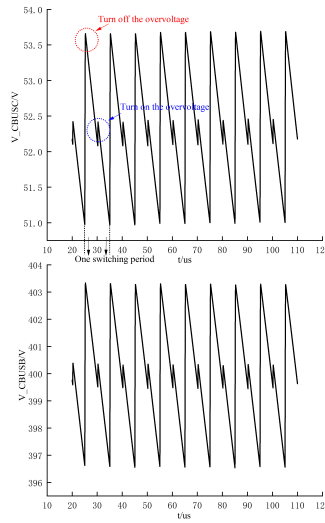
### 3.3.2 | Damping circuit resistance $R_{BS}$ and capacitance $C_{BS}$ value:

For setting the damping part, according to the analysis above, the resistor  $R_{BS}$  should be selected as large as possible to ensure that its influence on the half-bridge circuit is minimized when the half-bridge is turned on, but the value should not be too large to prevent the damping circuit from decoupling from the half-bridge circuit.

For the choice of capacitor  $C_{BS}$ , the analysis of equivalent Fig. 6 shows that its capacitance needs to be one order of magnitude higher than the parallel equivalent capacitance of the output capacitor  $C_{OSS}$  of SiC MOSFET and the parasitic capacitor  $C_D$  of diode  $D_s$ . A good damping effect can be achieved by setting  $R_{BS}$  to  $20\Omega$  and  $C_{BS}$  to  $10\text{ nF}$ .

### 3.3.3 | Absorption circuit capacitors $C_{BUSB}$ , $C_{BUSC}$ :

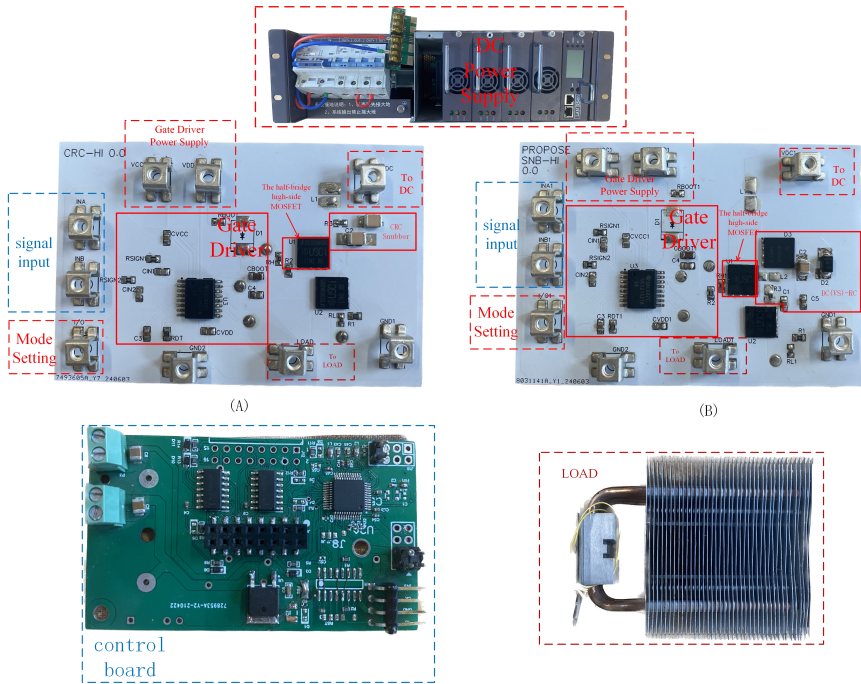
$C_{BUSB}$  and  $C_{BUSC}$  are set to  $200\text{ nF}$  and  $500\text{ nF}$ , respectively. In the design, it should be noted that the value of  $C_{BUSC}$  is much larger than that of  $C_{BUSB}$  to prevent excessive overvoltage energy from being absorbed by  $C_{BUSB}$  when overvoltage is absorbed, which will lead to excessive voltage oscillation of the upper and lower capacitors. Fig. 9 shows the voltage waveforms of  $C_{BUSB}$  and  $C_{BUSC}$  with this design. Among them, the voltage fluctuation of  $C_{BUSB}$  ranges from  $6\text{ V}$  to  $7\text{ V}$ , and that of  $C_{BUSC}$  ranges from  $4\text{ V}$  to  $5\text{ V}$ . Observing this waveform diagram, in a switching cycle, two voltage waveforms will appear two spikes, which are the overvoltage absorption phase of half-bridge off and half-bridge on.



**FIGURE 9** Absorption circuit capacitor voltage waveform

## 4 | EXPERIMENTS AND RESULTS

To verify the DC(VS)-RC absorption topology of the proposed SiC MOSFET, an experimental setup was built and a comprehensive comparative study was conducted. In Fig. 10, it is shown that experimental circuits with DC(VS)-RC and CRC buffer circuits are designed and tested. The printed circuit board is composed of a half-bridge part (including two half-bridge circuits with DC(VS)-RC and CRC buffer circuits), a driving circuit part, and a control circuit part. Table 1 gives the data of the component in the experimental setup.



**FIGURE 10** Experimental setup (A) half-bridge with RC snubber board (B) half-bridge with the DC(VS)-RC board.

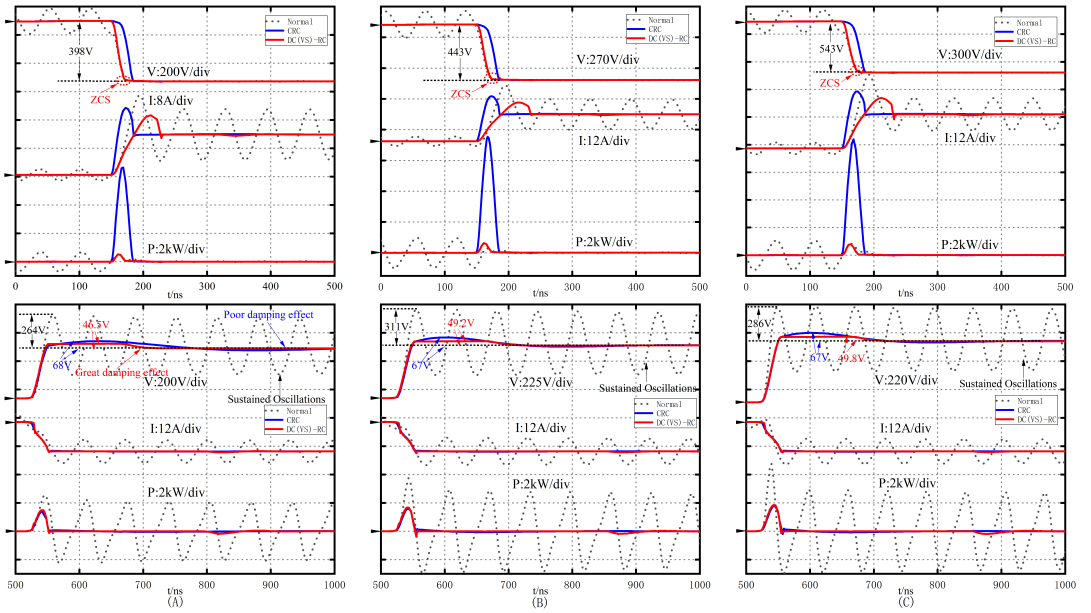
**TABLE 1** COMPONENT DATE IN THE EXPERIMENTAL SETUP

Components	Values	Descriptions
SiC MOSFET	650 V, 18 A	UF3SC065040D8S from UnitedSiC
$R_{BS}$	20 $\Omega$	0805 resister from Yageo
$C_{BS}$	10 nF	MLCCs from KEMET
$D_S$	650 V, 21 A	IDL02G65C5
$C_{BUSC}$	500 nH	MLCCs from KEMET
$C_{BUSB}$	200 nH	MLCCs from KEMET

#### 4.1 | Comparison Studies

In this part, the proposed DC(VS)-RC, CRC buffer circuits, and the half-bridge circuit without additional buffer circuits are compared and analyzed in detail. In PCB design, the half-bridge circuit board with buffer circuit should combine the buffer circuit with the switching devices as closely as possible to reduce the parasitic parameters of the buffer circuit. For the half-bridge circuit with CRC and without additional buffer circuit, the inductance of its bus feed loop is kept below 400 nH in this experiment, while for the half-bridge circuit with the proposed DC(VS)-RC absorption topology, an auxiliary inductance is added to the side of the feed loop close to the buffer circuit to make its loop inductance reach about 1.2  $\mu$ H.

Fig. 11 shows a typical waveform comparison (tested at a load current of 12 A and DC bus voltages of 400 V, 450 V, and 500

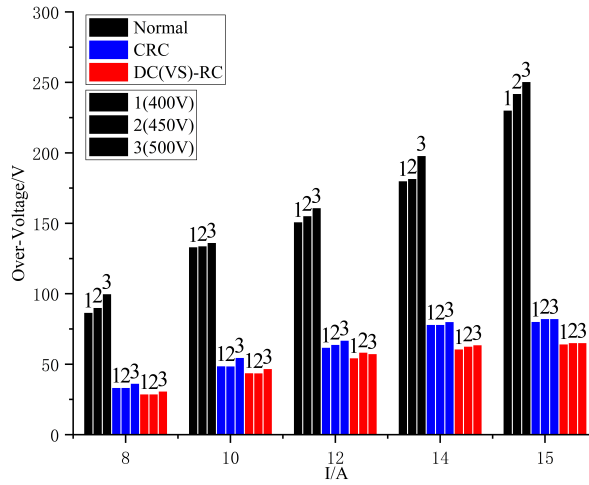


**FIGURE 11** Waveforms comparisons under 12 A, dc bus voltage at (a) 400 V, (b) 450 V, and (c) 500 V. (Figures above are turn-ON processes, figures below are turn-OFF processes).

V), the drain-source voltage  $V_{ds}$ , drain current  $I_d$  and power loss P of SiC MOSFET at the upper half bridge circuit are included. The upper part of Fig. 10 shows the turn-on point of the SiC MOSFET on the upper side of the half-bridge circuit, and the lower part shows the turn-off point. Fig. 10(A) shows that the ordinary circuit without buffer circuit has obvious overvoltage and oscillation, which will reduce voltage utilization, reduce the reliability of SiC MOSFETs at the turn-off point, and incur greater shutdown losses. Both the proposed circuit and the CRC buffer circuit are effective in solving these problems. The designed DC(VS)-RC circuit has an overvoltage of 46.5 V. The oscillation convergence is faster and slightly better than that of the CRC buffer circuit. SiC MOSFETs with the proposed circuit and the CRC buffer circuit applied have very close turn-off losses of 35  $\mu$ J and 33  $\mu$ J, respectively. From Fig. 10(A), it can be seen that during the power-up process,  $V_{ds}$  basically remains at the bus voltage until the voltage drop cycle starts due to the effect of the CRC buffer circuit. The turn-on loss of the SiC MOSFET with the RC buffer circuit is 157  $\mu$ J. This is much higher than the turn-on loss of 11.5  $\mu$ J and 7.6  $\mu$ J of the SiC MOSFET with the normal circuit and the proposed buffer circuit. This result verifies that the CRC buffer circuit will lead to an increase in the conduction loss, and since the switching loss of SiC MOSFET is mainly concentrated in the turn-on loss, the larger conduction loss leads to a sharp increase in the switching loss of SiC MOSFET. For the DC(VS)-RC buffer circuit, the auxiliary inductor is well used to realize the switching of the ZCS, and handle overvoltage and oscillations and reduce the total loss of the switching device. Similar results are reflected in Fig. 10(B) and (C).

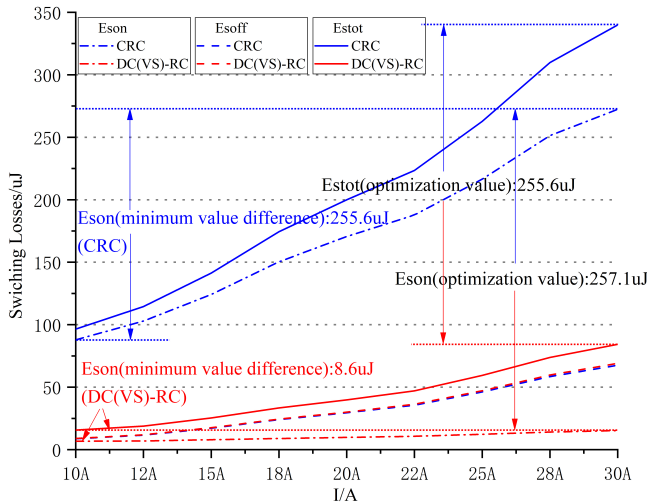
Fig. 12 shows the overvoltage comparison. After the load current is greater than 15A, the overvoltage value of the half-bridge circuit without buffer circuit has reached an unacceptable magnitude, which effects the safe and stable working of SiC MOSFETs. Under different conditions, the maximum voltage of DC(VS)-RC buffer is close to that of the CRC buffer, and both methods work well to suppress overvoltage and oscillations. Overall observation shows that the DC(VS)-RC buffer circuit is slightly better than the CRC buffer circuit.

Fig. 13 shows the detailed loss comparison at the condition of 400 V bus voltage. The comparison shows that for the



**FIGURE 12** Turn-OFF overvoltage comparison. (Marks 1, 2, and 3 represent tests at 400, 450, and 500 V, respectively).

turn-off loss  $E_{\text{soff}}$ , the  $E_{\text{soff}}$  of DC(VS)-RC is similar to that of CRC buffer circuit, and the amplitude changes with the increase of load current are small. However, for the turn-on loss  $E_{\text{son}}$ , when the load current is 10 A, the  $E_{\text{son}}$  applied with CRC buffer circuit is about 10 times that of the DC(VS)-RC buffer circuit, and with the increase of the load current, the  $E_{\text{son}}$  applied with CRC buffer circuit has a large fluctuation range. Increasing the load current from 10 A to 30 A results in a 255.6  $\mu\text{J}$  increase in  $E_{\text{son}}$ , and the fluctuation amplitude of  $E_{\text{son}}$  is very low for the DC(VS)-RC buffer circuit. This also makes the analysis of the overall loss  $E_{\text{stot}}$ , it can be concluded that the DC(VS)-RC buffer circuit has better performance than the CRC buffer circuit in the loss optimization of the half-bridge circuit.



**FIGURE 13** Losses comparison under 400 V dc bus voltage.

4.2 | Discussions

The comparison of the cost, performance and design difficulty of the design scheme is shown in Table 2.

- 1. Cost: Compared with other typical buffer circuit cost schemes, the DC(VS)-RC buffer circuit is close to the CRC scheme in terms of component cost. However, in the PCB design stage, because there is no need to optimize the loop inductance, it does not need to use multi-layer circuit board, only single-layer aluminum substrate or double-layer plate can be used. This greatly reduces the cost of the printed circuit board, and since the DC(VS)-RC buffer circuit can transfer the overvoltage energy, the heat dissipation requirements of SiC MOSFETs are reduced. AGD requires additional driver circuits, sensing circuits, and control circuits, which will also increase the cost.
- 2. Performances: DC(VS)-RC buffer circuit and AGD can reduce the switching loss of SiC MOSFETs while reducing the oscillation. However, the CRC buffer circuit and the scheme of optimizing the loop inductance cannot optimize the switching loss.
- 3. Design Difficulty: The design of passive buffer circuit including optimized loop inductor is easier than AGD design.

TABLE 2 Caption

Method	Cost	Performances	Design Difficulty
DC(VS)-RC	Moderate	High-level	Inferior
CRC	Inferior	Moderate	Inferior
Optimized Lloop	Moderate	High-level	High-level
AGDs	Moderate	High-level	High-level

5 | CONCLUSION

In this paper, a DC(VS)-RC buffer circuit topology applied to SiC MOSFET half-bridge circuit is designed and proposed. Through theoretical and experimental analysis, the DC(VS)-RC buffer circuit has the following characteristics:

- 1. By using the placement auxiliary inductor, the SiC MOSFET achieves ZCS zero-current turn-on, which greatly optimizes the turn-on loss of SiC MOSFET.
- 2. The DC(VS)-RC buffer circuit can effectively suppress overvoltage and oscillation in both turn-on and turn-off phases.
- 3. The absorption circuit is divided into two capacitors, one is used to pull the voltage of the raise capacitor, and the other is used as the clamp capacitor to absorb the overvoltage to reduce the scale for subsequent energy transfer. The turn-OFF overvoltage and oscillation energy stored in the clamp capacitor can be fed back to the DC bus. Meanwhile, the absorption and feedback loss of DC(VS)-RC are very low.

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