Investigation of β-Ga_2O_3-based HEMT for Low Noise Amplification and RF Application

R. Singh[1], T. R. Lenka[1], D. K. Panda[2], and H. P.T. Nguyen[3]

***Abstract*—**Here we demonstrate a two-dimensional β-gallium oxide-based high electron mobility transistor (HEMT) comprising of a finite gap—access region gap (L_{ARG}) in Ohmic-contact access regions with record transconductance linearity. Apart from limiting two-dimensional electron gas (2DEG) density n_s dependency on gate voltage, higher saturation current is estimated for the proposed design. Since the access regions length directly affects the Capacitance of the device and resultant switching applications. In this work, the effect of the gate-source and gate-drain length on device linearity is performed using Atlas-2D simulations. $C-V$ characteristics of the proposed device are explained based on the physical explanation and validated using appropriate models. The higher values of transconductance g_m and current gain cut-off frequency f_T on a large span of operating voltages ensure improved transistor performance for low-noise amplification and RF application and are reported for the first time.

***Index Terms*—**2DEG, AlN/β-Ga_2O_3, access-regions, Capacitance, $C-V$ characteristics, Gaussian-doping, HEMT, linearity, quasi-saturation, source-resistance, transconductance.

I. INTRODUCTION

High-electron-mobility-transistors have shown outperformance in terms of high-frequency and high-voltage operations. Higher two-dimensional-electron gas (2DEG) density n_s ~ 10^{12}-10^{13} cm^{-3} and 2DEG mobility of 1200-1500 cm^2 $V^{-1}s^{-1}$ make GaN-based HEMTs the preferable choice for high-frequency electronics applications. However currently, a relatively new semiconductor material gallium-oxide (Ga_2O_3) is being explored at a fast pace for potential high-power and high-frequency electronics emerging applications. Out of its five phases, the β-phase is found to be the most stable and has some interesting properties like large bandgap E_g ~ 4.5-4.9 eV, critical electrical field E_C ~ 8-9 MV/cm, and availability of economical single crystal substrates grown using melt-based growth techniques [1]–[4]. Despite the low electron mobility μ_n ~ 150-200 cm^2 $V^{-1}s^{-1}$ issue, researchers have shown enough pieces of evidence that Ga_2O_3 can complement existing GaN and SiC technology [5]–[7].

Despite high carrier density and carrier velocity, HEMTs generally suffer from nonlinearity issues. The gain i.e. transconductance g_m, and current-gain cut-off frequency f_T, after reaching their peak values, show a rapid fall with gate bias [8], [9]. This bias-dependent nonlinearity affects the noise performance of amplifiers and is attributed to the high resistivity of Ohmic-contact access regions. Several methods have been proposed so far to ease this effect using high-doping in the source-access region at the heterointerface [8], and multi-channel structures [10], [11] and achieved good linearity by reducing access-region resistance. Earlier this was explained based on enhanced electron-phonon interactions in GaN HEMTs [9]. Lately, several three-dimensional (3D) structures are proposed comprising 3DEG [12], and lateral-gated 3D structures like junction field-effect transistors (JFETs) with lateral depletion [13]. Few of them have lower breakdown voltage while most have sophisticated designs.

Access region resistance has been identified as the main source of nonlinearity in high-electron-mobility transistors (HEMTs), and surface potential based analytical model and its temperature dependence for GaN based HEMT has been reported [14], and experimental analysis of source resistance in InGaAs/InAlAs HEMTs [15]. Furthermore, parasitic source resistance was measured based on varying gate bias and gate length of GaN based heterostructure FETs (HFETs) [16], and optimization of nonlinear access resistance in β-Ga_2O_3 based HEMTs has been reported [17]. These various methods envisaged to minimize dynamic access resistance broadly ranges from high-doping in the access region and three-dimensional structure comprising three-dimensional electron gas (3DEG) and lateral depletion. However, the effects of a particular method proposed for reducing access resistance on the capacitances and resulting linearity of the device require more investigation.

In this paper, TCAD simulations have been performed, on a β-Ga_2O_3 HEMT with access-region-gaps, to quantify the effects of varying access-region lengths on the $C-V$ behavior and linearity of the device. The $C-V$ behavior is validated by appropriate analytical models reported earlier. The Section II explains device structure and simulation outline followed by results and discussion in section III. The paper is concluded in Section IV.

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II. DEVICE DESIGN AND SIMULATIONS FRAMEWORK

The schematic of the device under test is shown in Fig. 1 (a). The epitaxial layer sequence consists of 50-nm width β-Ga_2O_3 buffer layer on a semi-insulating β-Ga_2O_3 substrate, followed by 10-nm width AlN barrier layer. The buffer layer has a doping concentration of 10^{16} cm^{-3}, while the barrier layer is undoped. The gate contact is Schottky type, while drain and source contacts are the Ohmic types with a contact resistance of 0.4 ohm-mm as given in [18]. The device has the gate-length L_G of 0.1 µm, and equal gate-source L_{GS} and gate-drain length L_{GD} of 0.7 µm. The AlN barrier is contracted laterally to create a finite gap—access region gap L_{ARG} of 0.05 µm. This is done to minimize charge depletion in the vicinity of barrier end and source/drain regions. The same can be done easily using more popular self-aligned technology, which is leveraged here for potential gain in device linearity. The schematic of conventional HEMT, used for comparing results, is also shown in Fig. 1 (b). The device width is set as 50 µm and all the reported quantities are normalized on this dimension. All simulations and numerical computations are performed using ATLAS 2D device commercial software [19], and MathWorks - MATLAB [20] respectively. For a drain bias up to 15 V, and a critical field of 1.54 kV/cm [21] the ratio V_{DS}/E_C is equal to 1 µm. Therefore to keep the maximum electric field in access regions below E_C, the overall lateral length of the device i. e. source-drain distance L_{SD} is kept at 1.5 µm.

The β-Ga_2O_3 material parameters such as energy bandgap E_G, conduction and valence-band density N_C and N_V, dielectric permittivity ε_r among others are taken from [4], [22]. The duo polarization models—spontaneous and piezoelectric are enabled for AlN material as provided in [19]. To capture the carrier velocity saturation effect in the β-Ga_2O_3 channel, a field-dependent mobility model is invoked among others like Shockley-Read-Hall (SRH) recombination, and Fermi Dirac statistics for carrier concentration. The user-defined parameters are given in Table 1, while the rest all for materials and models are used as default given in [19]. To capture the velocity saturation effect in velocity-field characteristics, a negative differential mobility model as given in [19] is used and default model parameters are replaced by values reported in [21].

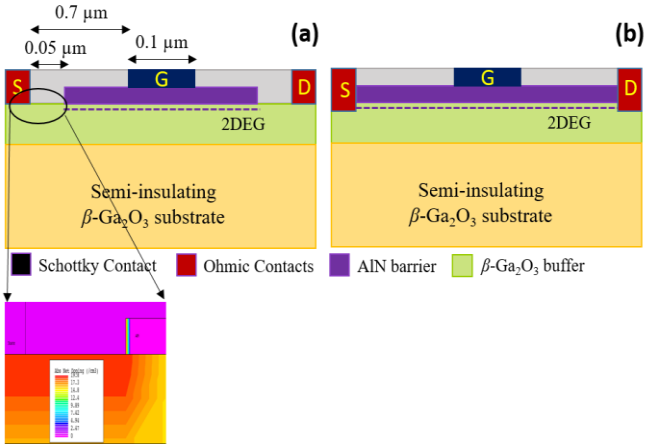

Fig. 1. Schematic view of the AlN/β-Ga_2O_3 HEMT device structures **(a)** device under test, Enlarged: Gaussian doping extending from Ohmic-contact to barrier edge **(b)** conventional HEMT, Ohmic contacts extended up to few nm in barrier layer (Dimensions not scaled)**.**

$$\mu_n(E) = \frac{\mu_0 + \frac{v_{sat}}{E}\left(\frac{E}{E_C}\right)^{\gamma}}{1 + \left(\frac{E}{E_C}\right)^{\gamma}} \tag{1}$$

Table I
β-Ga_2O_3 material and parallel field mobility model parameters

Symbol	Quantity	Value (unit)
$\mathcal{E}_g$	Energy bandgap	4.9 eV
$\mathcal{N}_C$	Conduction band density	3.6×10^{18} cm^{-3}
$\mathcal{N}_V$	Valence band density	2.86×10^{20} cm^{-3}
χ	Electron affinity	3.15 eV
ε_0	Static dielectric constant	10
μ_0	Low field mobility	140 cm^2 V^{-1} s^{-1}
v_{sat}	Saturation velocity	1.5×10^7 cm s^{-1}
$\mathcal{E}_C$	Critical field	1.54×10^5
γ	Constant	2.47

III. RESULTS AND DISCUSSION

A. Limit to Linearity

Since in HEMT, 2DEG density n_s has a profound effect on device operation and is a complex function of gate voltage. So it is vital to consider this bias-dependent behavior of 2DEG density in linearity analysis of the HEMTs. The explicit relation between n_s and V_{GS}, as given in [23], can be written as follows:

$$n_s(V_{GS}) = \frac{C_g V_{g\_eff}}{q} \frac{-\frac{\gamma_0}{3}\left(\frac{C_g V_{g\_eff}}{q}\right)^{2/3}}{V_{g_{eff}}\left(1 + \frac{V_{th}}{V_{g_{eff_d}}}\right)} + \frac{2}{3}\gamma_0\left(\frac{C_g V_{g\_eff}}{q}\right)^{2/3} \tag{2}$$
$$V_{g_{eff}} + V_{th}\left[1 - ln\left(\beta V_{g_{eff_n}}\right)\right]$$

where, $C_g = \epsilon_{AlN}/d_{AlN}$ is the gate-capacitance, $V_{g\_eff} = V_{GS} - V_{OFF}$ is the effective gate voltage, V_{th} is the thermal voltage 0.0259 V at 300K. $V_{g\_eff\_n}$, $V_{g\_eff\_d}$ are functions of V_{g_eff} is given as $V_{g\_eff}\left(\alpha_x/\sqrt{V_{g\_eff}^2 + \alpha_x^2}\right)$, where $\alpha_n = \exp(1)/\beta$, $\alpha_d = 1/\beta$, and $\beta = C_g/qDV_{th}$, where D is the density of states. The 2DEG density n_s is numerically computed using MATLAB and plotted against V_{GS} for the proposed AlN/β-Ga_2O_3 HEMT as shown in Fig 2. It can be seen that 2DEG density rises vertically once $V_{GS} > V_{OFF}$ and gradually saturates for higher gate voltages. As n_s increases, electron effective velocity decrease as $v_{eff} \sim 1/\sqrt{n_s}$ and subsequently a similar drop in values of g_m and f_T can be expected due to quasi-saturation of electron velocity [8], [9]. This bias-dependent effect of n_s on V_{GS} looks more evident in submicron devices as L_{GS} is kept short for optimum RF performance. To circumvent this n_s variation in the channel ends near source/drain contacts, highly doped (Gaussian-type), finite access-area gaps L_{ARG} have been introduced in the proposed design. This is validated based on the variation in carrier density versus V_{GS} for different L_{ARG} using TCAD simulations and is shown in inset of Fig. 2.

The results obtained are on the expected lines. The intensity of bias dependent behavior of n_s with V_{GS} significantly reduces and becomes constant beyond V_{GS} = 2 V for all values of L_{ARG}. Therefore, it can be concluded that in access regions, higher values of L_{ARG} pointedly restricted percentage rise in carrier concentration with increasing gate voltages.

The $I_D - V_{DS}$ characteristics of the proposed as well as conventional HEMTs are shown in Fig. 3. Maximum drain current I_{DMAX} of 0.32 and 0.1 A/mm is found for the device with L_{ARG} and conventional one respectively. Over 200 % rise in saturation current is observed for the proposed device. This is attributed to bias-independent high doping in source/drain access regions. Moreover, lower values of ON-resistance R_{ON} corresponding to the proposed device over conventional structure ensure lower net conduction losses. Furthermore, the lower knee voltage provides a large output voltage swing.

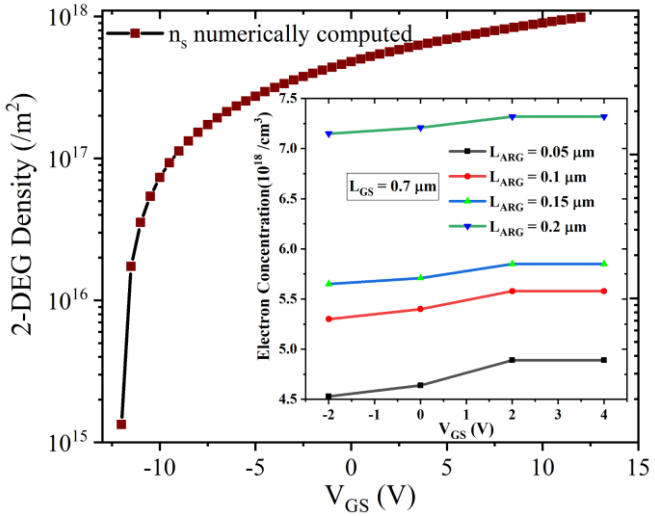

Fig. 2. Variation of 2DEG density n_s versus gate-voltage V_{GS} for proposed HEMT design. Inset: Effect of change in L_{ARG} on electron concentration in source access region. The rate of increase in n_s comes down with increase in L_{ARG}.

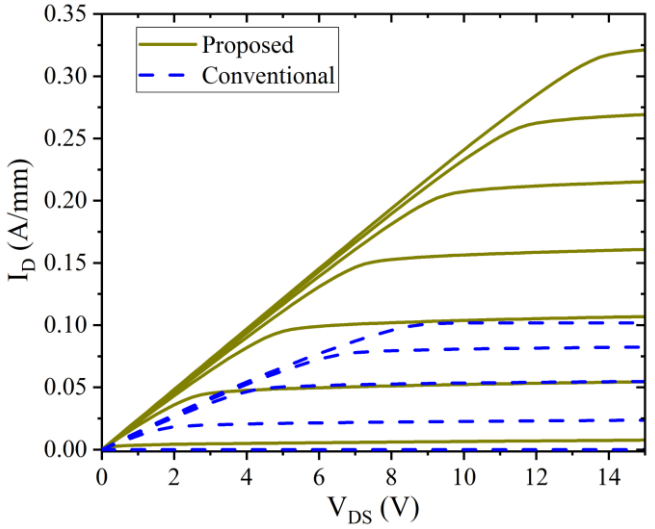

Fig. 3. $I_D - V_{DS}$ characteristics of the proposed and conventional HEMT designs, V_{GS} is varied from –12 to 0 V and –8 to 0 V in step of 2 V.

B. Effect of Access Region Length

As the access region length changes, the overall access resistance also changes. To evaluate the effect of the access region lengths on the linearity of the device, two different cases have been considered. In the first set of simulations, L_{GS} decreases, and L_{GD} increases in the step of 0.2 μm keeping the L_{SD} constant, while in the second one, only L_{GS} is decreased keeping L_{GD} constant. The resultant effects on output current and gate-capacitances with varying gate voltage from –15 to 1 V are analyzed. A drain bias of 15 V is pre-applied to get the I_D–V_{GS}, and $g_m - V_{GS}$ characteristics of the devices. The extracted values of gate-source and gate-drain capacitances C_{GS} and C_{GD} have been used for the physical explanation of the device linearity. From Fig. 4, it can be seen that access region length significantly affects the drain current I_D and so the transconductance g_m.

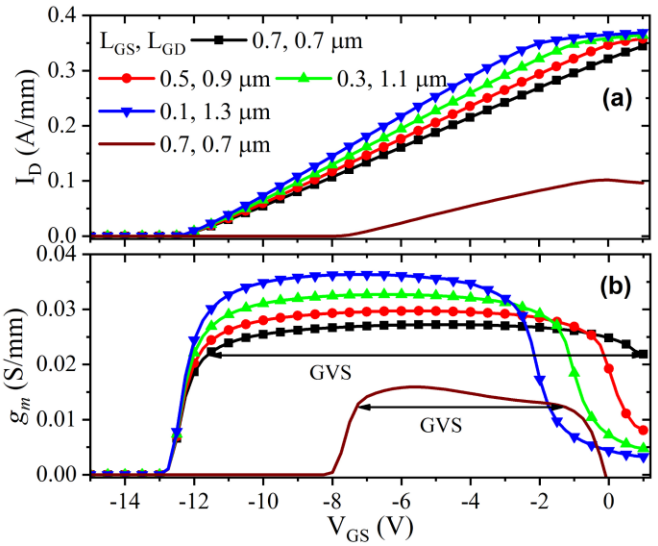

Fig. 4. Effect of varying L_{GS} and L_{GD} on drain current and transconductance of proposed device, L_G = 0.1 μm for all cases. **(a)** I_D – V_{GS} **(b)** g_m – V_{GS} characteristics. Line plus symbols are used for proposed device and only line for conventional. Common legends are used. GVS is mentioned to evaluate linearity.

As L_{GS} reduces, lower source-access resistance facilitates higher I_D. Although at higher V_{GS}, the drain current starts to saturate. This can be attributed to increased drain-access resistance since L_{GD} keeps increasing. The electric field peak now occurs in the higher resistive drain-access region. This observation is in good agreement with the explanation given in [24]. The linearity of the devices is evaluated based on transconductance curves. A Figure of Merit (FOM)—gate voltage swing (GVS) defined as voltage range for which transconductance does not fall below 20 % of maximum value, is used to measure linearity [13]. For the proposed device, it is measured as greater than 12 V which is 100% higher than its respective value of 6 V for conventional HEMT. The maximum value of transconductance increases as L_{GS} decreases, although GVS decreases due to the high resistivity drain-access region as explained earlier and found in good agreement with the phonon-model as explained in [9].

In the second case of analysis, L_{GS} reduces as explained earlier but now L_{GD} is fixed. The appropriate change in L_{SD} is obvious and is incorporated to fit these settings. The resultant effects on I_D and g_m are shown in Fig. 5. Due to reduced source-access resistance and constant drain-access resistance, here

drain current I_D increases proportionally and negligible saturation at higher gate voltage. Consequently, almost flat curves of transconductance g_m with GVS of 12 V are measured. These results and observations are endorsed by C–V characteristics of the proposed device and are given in the next subsection. The gate-source and gate-drain capacitances C_{GS}, and C_{GD} are further validated based on appropriate analytical models.

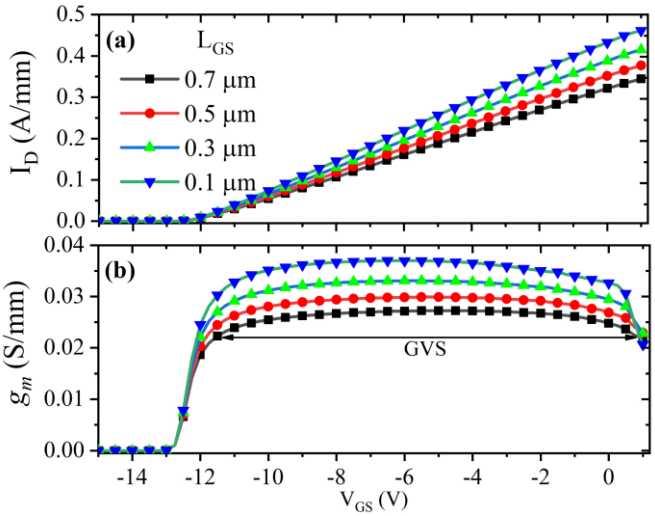

Fig. 5. Effect of varying L_{GS} on drain current and transconductance of proposed device, L_G = 0.1 and L_{GD} = 0.7 μm is fixed. **(a)** $I_D - V_{GS}$ **(b)** $g_m - V_{GS}$ characteristics. Common legends are used. GVS is almost constant even for higher transconductance value curves.

C. C – V Analysis

Since the access region length significantly affects $C-V$ characteristics of the device, small-signal capacitance-voltage analysis is done at a frequency of 1 MHz after applying a drain-bias of 15 V. Gate capacitances C_{GS} and C_{GD} are extracted as a function of varying V_{GS} and are shown in Fig. 6 and Fig.7.

As V_{GS} increases slightly above the cut-off voltage V_{OFF}, C_{GS} values rise vertically and are attributed to the dependence of electron concentration in the channel on V_{GS} as explained in subsection A. It can be seen from Fig. 6 that for all V_{GS} beyond V_{GS}, C_{GS} increases monotonically with decreasing L_{GS}, and increasing L_{GD} and plateau is observed. Although a small increase in C_{GS} values are observed at higher V_{GS}, corresponding to L_{GD} = 1.1 and 1.3 μm, as shown in inset Fig. 6 a. This behavior can be explained on the physics-based compact models as given in [25], [26]. Since the 2DEG density is strong in this region, total gate-capacitance C_G is equal to channel capacitance C_{CH} which is defined as $q\,dn_s/dV_G$ [25]. It is important to note that due to the doped β-Ga_2O_3 buffer layer ($N_D = 10^{16}$ cm^{-3}), these doped charges are also added to C_G. Now, $C_G = C_{CH} + C_{DEP}$, and deletion capacitance is defined as $C_{DEP} = C_{DEP0}/\left(1 + V_{bi}/V_{g,eff}\right)^{1/m+2}$ where V_{bi} is the built-in voltage and $C_{DEP} = C_{DEP0}$ for $V_{g,eff} > V_{bi}$, and m is the doping profile dependent parameter [25]. Based on this model, it is obvious that as L_{GD} increases more depletion charges are added up to the C_{GS} at higher V_{GS}. On the contrary, there is no such divergence in the $C_{GS} - V_{GS}$ characteristics for the second set of analyses is observed, where the L_{GD} is kept constant (Fig. 6 b).

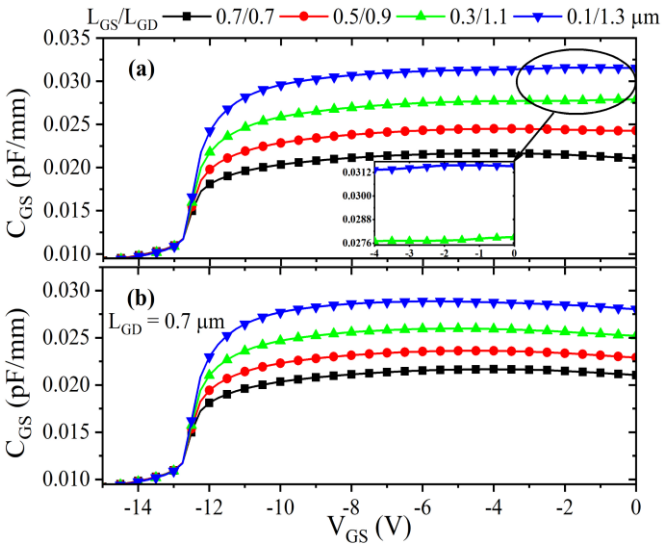

Fig. 6. Effect of changing access lengths on $C_{GS} - V_{GS}$ characteristics of the proposed device with fixed L_G = 0.1 μm. **(a)** Both L_{GS} and L_{GD} are changed in the step of 0.2 μm, Inset: small increase in $C_{GS} - V_{GS}$ (– 4 to 0 V) relating to L_{GD} = 1.1 and 1.3 μm is highlighted **(b)** Only L_{GS} is changed and L_{GD} is fixed. Common legends are used.

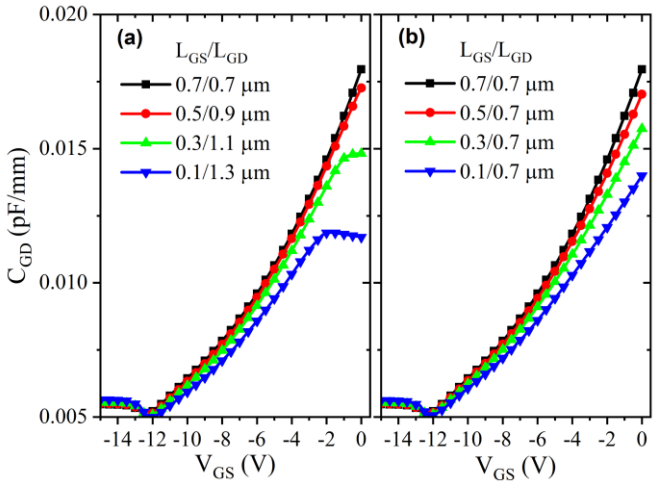

Fig. 7. $C_{GD} - V_{GS}$ characteristics for the proposed device. **(a)** Both L_{GS} and L_{GD} are varied in tandem. **(b)** Only L_{GS} is changed, L_{GD} is fixed. In both cases peak value of C_{GD} decreases with L_{GS} scaling, however for L_{GD} = 1.1, 1.3 μm, C_{GD} starts to decrease at higher V_{GS}.

Gate-drain capacitance versus gate voltage for varying access region length is shown in Fig. 7. From both the plots, it can be seen that C_{GD} increases with increasing V_{GS}, but the peak value decreases with reducing L_{GS}. This can be attributed to the rising values of C_{GS} values with increasing V_{GS} as explained previously based on the analytical model [25] and since total gate-capacitance $C_G = C_{GS} + C_{GD}$. Furthermore, for the first case corresponding to L_{GD} = 1.1 and 1.3 μm, C_{GD} starts to decrease beyond - 3V of V_{GS}, as shown in Fig. 7a. This can be attributed to poor control of the drain electrode as L_{GD} increases. It is validated by invoking the capacitance model [26], and simulations are performed to verify the dependence of C_{GD} on V_{DS} for various values of V_{GS}. The plots shown in Fig. 8 are in good agreement with related findings in [26].

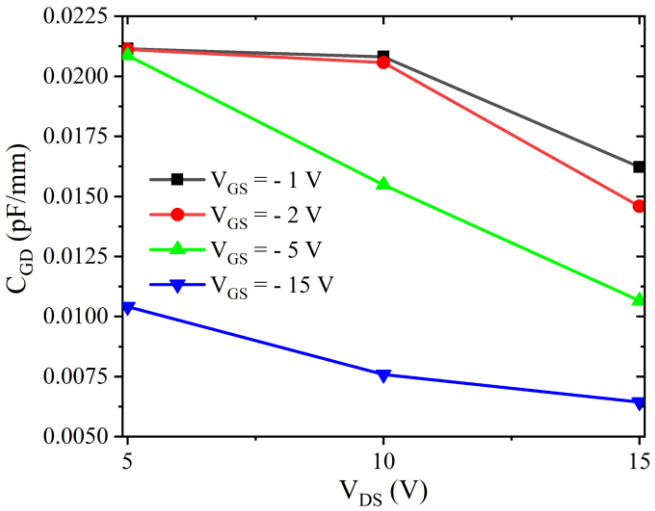

Fig. 8. Effect of higher drain bias on C_{GD} at fixed V_{GS}. Gradual decrease of C_{GD} with increasing V_{DS} can be interpreted as steady loss of drain electrode control over channel charge. This is in-line with the capacitance model in [26].

D. RF Performance

In order to evaluate the RF performance of the proposed device, a small-signal high-frequency analysis is performed based on the respective simulated transconductance curves. The cut-off frequency f_T, and associated maximum oscillation frequency f_{MAX} are extracted from the simulated current-gain h_{21} and unilateral power gain U versus frequency characteristics. Fig. 9 shows the simulated values of cut-off frequencies versus gate-voltage. It can be seen that f_T dependence on V_{GS} follows a similar trend as transconductance, but with limited linearity. The peak value of f_T is found to be 170 GHz which gradually decreases with increasing V_{GS}. The fall in f_T can be attributed to increasing gate-drain capacitance C_{GD} as shown in Fig. 7. The cut-off frequency f_T is also calculated based on the following relation:

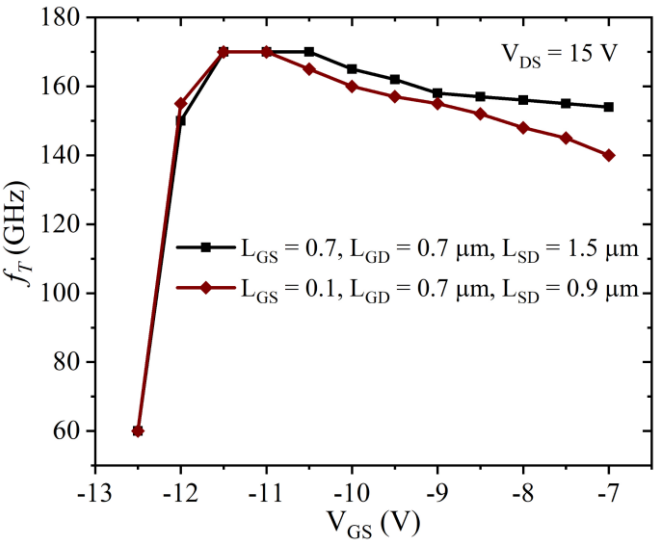

Fig. 9. Plot of extracted cut-off frequency f_T versus gate voltage V_{GS} at V_{DS} = 15 V of the proposed device with gate-length L_G = 0.1 µm.

$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})} \quad (3)$$

Numerically computed values of f_T using (3) are found to be slightly lower than the simulated values, nevertheless follows the similar trend with gate voltage.

IV. CONCLUSION

The inherent factors limiting the linearity performance of HEMTs are analyzed qualitatively. Simulation results of the proposed HEMT design, which incorporate measures to circumvent these issues, have shown excellent transconductance linearity and moderate cut-off frequency linearity as a function of increasing gate voltage. The effect of varying access region length on the $I_D - V_{GS}$ and $g_m - V_{GS}$ characteristics are thoroughly investigated. These DC characteristics are explained based on capacitance-voltage measurements which are validated by appropriate physics-based analytical models. Apart from inherent advantages like simpler design and negligible parasitic capacitances of the planar HEMT, the proposed design equipped with better linearity is expected to be useful in low-noise amplifiers and RF applications.

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