A 1.2V High-speed Low-power Preamplifier Latch based Comparator

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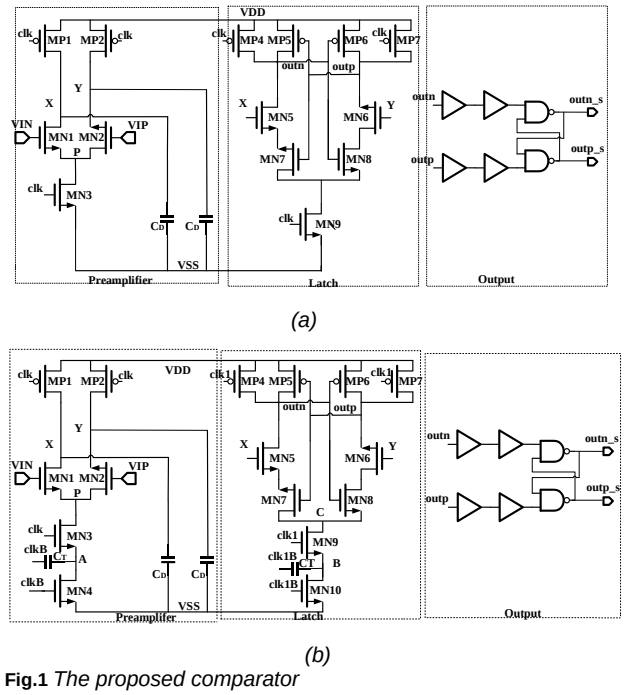
The power consumption of chips has emerged as a major concern with the increased integration of analog circuitry. This work focuses on a two-stage comparator based on a preamplifier with latch for successive approximation analog-to-digital converter. In order to minimize power loss and delay time, the charge steering approach was used in the design of latch as well as preamplifier. The suggested comparator is simulated in SMIC 0.18um process in comparison to the comparator without charge steering mode. The results reveal that the average power consumption is only around 22uW for varied input voltage at a supply voltage of 1.2V, which is relatively lowered by approximately 30%. Meanwhile, delay time is also reduced by about 25%.

Introduction: A wide range of mobile computing devices and health care applications currently require the use of successive approximation analog-to-digital converters (SAR ADC) [1,2]. Low-power designs have developed into a significant trend due to the growing integration of analog circuitry. Preamplifier Latch based Comparator is the primary component of SAR ADC, which play a crucial function by being able to transform tiny analog signal voltages into digital signals.

To solve the problem the preamplifier and latch stage's output node is fully discharged to ground at the conclusion of the comparison, which use up the majority of the comparator's power. [3-5]. The paper introduces a charge steering technique based on the study of the above problem. It is not only used for the preamplifier, but also for the latch by replacing the current sink at the tail with a capacitor at the charged sink. Compared to the comparator without charge steering mode, the simulation verification goes to determine whether the power consumption is improved.

Proposed design: The basic function of a comparator is to compare two analog input signals and output a binary signal based on the comparison result. The comparator consists of three parts: a preamplifier, a latch, and an output buffer, as shown in Fig. 1. The preamplifier is a circuit used to amplify the signal in order to drive the load. The latch is designed to speed up the output response of the comparison by using a back-to-back inverter. The main purpose of the output buffer is to convert the output signal of the latch circuit into a logic signal.



(a)

(b)

Fig.1 *The proposed comparator*

Firstly, the standard preamplifier [6] is a differential amplifier with an active load in Fig.1(a). Transistors MP1 and MP2 switch on when the clk drops during the reset phase, the pre-charging nodes X and Y to the supply voltage VDD. The capacitor C_D on nodes X and Y start to discharge until they reach zero during the comparison phase, when transistors MP1 and MP2 turn off. The difference between the drop in nodes X and Y is then transferred to the latch section, depending on the magnitude of the differential input voltages VIN and VIP. The output node capacitors (C_D) of the preamplifier are fully charged to the supply voltage VDD during this operation, and subsequently they are entirely drained to ground, using $2*C_D*VDD^2$ of energy for each comparison. The tail current source in this paper's charge steering mode[7] preamplifier is a partial charge for conversion rather than a constant current in Fig.1(b). The clock of clkB is high during the reset phase, capacitor C_T begins to charge, and transistor MN3 is turned off. The transistor MN3 conducts as the capacitor C_T begins to discharge while the clock of clkB is low, raising the voltage V_A at node A in the comparison phase. The gate source voltage of transistors MN1 and MN2 begin to drop as the V_A rises, and this decrease continues until voltage reaches the first burst point Vp=min (VIP-Vthn1, VIN-Vthn2). Another transistor keeps discharging the matching capacitor of C_D, until the voltage of the second quenching point Vp = max (VIP-Vth1, VIN-Vth2) is achieved. The threshold voltages of transistors MN1 and MN2 are Vthn1 and Vthn2, respectively. Voltage V_X/V_Y at the X/Y node does not reach zero at the conclusion of the comparison phase; rather, it

remains at a specific value. Therefore, energy consumption is [$2C_D$*VDD^2-VDD*C_D*(V_X+V_Y)], which is significantly lower than the energy consumed by a traditional differential amplifier.

To fix a problem: The preamplifier enters pre-charge mode and its differential output begins to crash as soon as the latch begins to sense [8]. Then, clkB and clk1B are the corresponding complementary signals to the two master clocks, clk and clk1, respectively. this clk1 is the post-delay signal of clk and permits off-chip calibration of the overlapping cycles when its delay time ranges between 35% and 60% of the clk cycle's high level. In Fig.1(b), during the reset phase of latch, clk1 is clocked low and transistors MP3 and MP7 are turned on, charging the nodes of outn and outp to the supply voltage VDD. Then transistor MN9 is turned off, separating the charge steering module from the latch section above. At the same time, C_T is also charged. In the comparison phase, clk is high and transistors MP3 and MP7 are all off. And transistor MN9 is on, which combines the charge steering module with the latch section above. At the same time, C_T is discharging, increasing the voltage Vc at the potential point C. When transistors MN5 and MN6 are on, a differential current proportional to that between Vx and V_Y is generated. The voltages at nodes outn and outp start to drop, the faster the node corresponding to the branch with the higher current drops until it is zero, and then another node is pulled to VDD. As for the power consumption, the latch achieves similar results as the preamplifier, which will not be elaborated here.

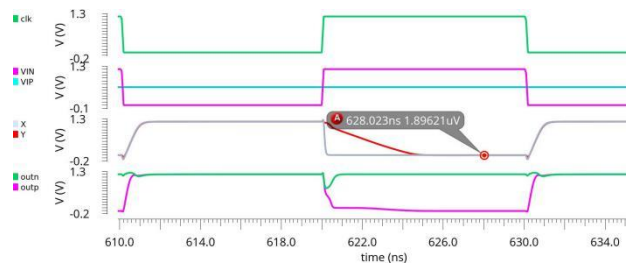
Secondly, about the aspect of latency time. The delay of a conventional latch is composed of two times delays, t_0 and t_{latch}. In the proposed latch, due to the capacitive charging of the load capacitance until the n-channel transistor (MN5/MN6) turns on. In this process, the time needed is called t_0, which is similar to the conventional latch. The t_{latch} is the time taken by a cross-coupled latch to regenerate output to settled values. Thus, the t_{latch} is given by [9].

$$t_{latch(a)} = \frac{C_{pL}}{g_{m,eff}} ln(\frac{\Delta V_{out,final}}{\Delta V_{out,t_0}}) = \frac{C_{pL}}{g_{m,eff}} ln(\frac{VDD}{\Delta V_{out,t_0}}) \quad [1]$$

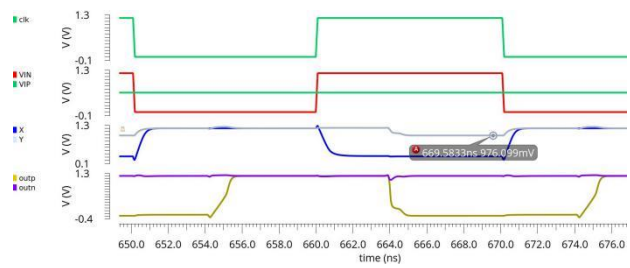
$$t_{latch(b)} = \frac{C_{pL}}{g_{m,eff}} ln(\frac{VDD - Vx}{\Delta V_{out,t_0}}) \quad [2]$$

where C_{pL} is the load capacitance of the latch; $g_{m,eff}$ is the effective transconductance of the back to back inverters; $\Delta V_{out,t0}$ is the initial difference between the output nodes just after amplification at time t_0; $\Delta V_{out,final}$ is the initial difference between the output nodes after the final of comparison, Vx is dropout value of output voltage in the proposed latch, which is very much larger than zero. Therefore, in the proposed latch, we reduce the delay time, that has the greatest impact on the total delay of the comparator.

Simulation results: One comparator without borrowing charge steering mode, named comparator I. The other comparator using charge steering mode is named comparator II. They are designed in the SMIC 180nm CMOS process. The supply voltage (VDD) is set to 1.2 V and the sampling rate is set to 100 MHz, and the designed circuits are simulated using the software of cadence. Fig.2 depicts the simulated timing waveform of two comparators, relatively. They are designed at the same square wave signals for the clk and VIN, VIP equal to 0.6 V and VDD equal to 1.2 V. As a result of the comparator I, at high values of the clk, the points of X and Y are very near to zero. Meanwhile, as a result of comparator II, at high levels of clk, the point of X is close to zero, whereas the point of Y is close to 987 mV for the same high level of clk. In this way, the previous theory is verified.

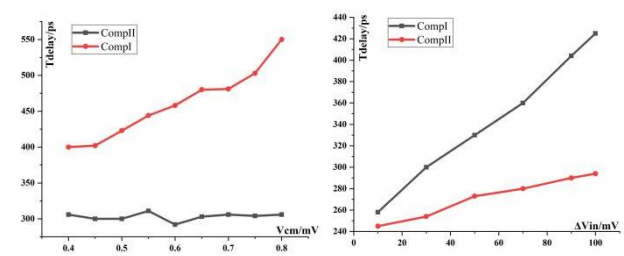


(a)



(b)

Fig.2 *The simulated timing waveform*

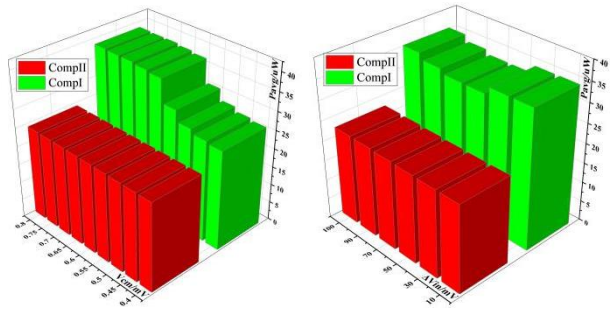


(a) (b)

Fig.3 The simulation results of delay time

The delay time (Tdelay) and average power consumption (Pavg) of these comparators are simulated for different values of common mode voltage (Vcm) and different values of input common Vin under Vcm equal to 600 mV.

Fig. 3 (a) and (b) present the simulation results of delay time. Obviously, the delay time of comparator II is at least 25% less than comparator I at different values of Vcm, and when Vcm is 600 mV, the delay time of comparator II is at its minimum. Fig. 4 (a) and (b) present the simulation results of the Pavg. The Pavg of comparator II is stable at about 22uW regardless of the variation of Vcm or Vin, and is about 30% less than comparator I.



(a) (b)

Fig.4 The simulation results of Pavg

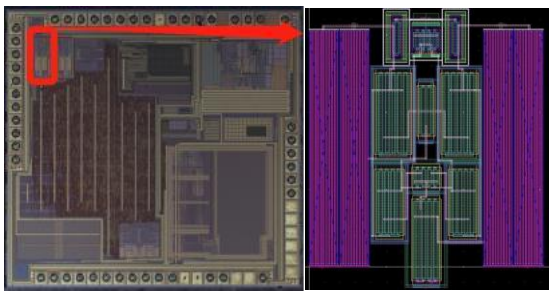


Fig.5 The layout

Table 1: Performance comparison

	[10]	[11]	[12]	This work
Power supply(V)	1.2	1.2	1.2	1.2
Process （um）	0.18	0.13	0.065	0.18
Delay time(ps)	388	239	120	292
Pavg(uW)	109	100	412	22

Finally, Fig. 5 presents the layout of the preamplifier and latch in the comparator II, which is designed to be symmetrically paired. The performance of the comparator II designed in this paper is compared with that of similar comparators in Table 1. As can be seen from the table, in comparison, although the latency is not the shortest, the Pavg is much reduced.

Conclusion: In this paper, a high-speed and low-power-consumption pre-latch comparator with charge steering mode for both pre-stage and latch stage circuits is designed. The simulation results show that the average power consumption is only around 22uW for varied input voltages at a supply voltage of 1.2V, which is relatively lower by approximately 30%, and delay time is also reduced by about 25%.

References

1. Yu jia Huang, et al.: A high-speed low-power SAR ADC in 40nm CMOS with combined energy-efficient techniques, IEICE Electron.Express18,2021
2. Takayuki OKAZAWA, Ippei AKITA: A Dynamic Latched Comparator Using Area-Efficient Stochastic Offset Voltage Detection Technique, IEICE Transactions on Electronics 5,2018
3. Y. B. Ni, et al.: A high speed dynamic comparator with low-power supply voltage, IEEE Solid-State Integrated Circuit (ICSIC),2018, pp. 1-3
4. A. M. Maghraby, et al.: A Low-Noise, Low-Power, Dynamic Latched Comparator Using Cascoded Structure, 2020 12th International Conference on Electrical Engineering (ICEENG), 2020, pp. 335-338
5. S. Tabassum, et al.: A low power preamplifier-latch based comparator using 180nm CMOS technology, IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia),2013
6. Rahmani, S, et al.: Design and analysis of a high-speed double-tail comparator with isomorphic latch-preamplifier pairs and tail bootstrapping, Analog Integrated Circuits & Signal Processing,2017, pp.507-521.
7. M. S. Eleraky, et al.: A low power Charge Steering Based Frequency Divider, National Radio Science Conference (NRSC) ,2020, pp. 197-206
8. M. M. Ayes, et al.: Design and analysis of a low-power high-speed charge-steering based Strong ARM comparator, 2016 28th International Conference on Microelectronics (ICM),2016, pp. 209-212
9. S.A. El-Sayed, et al.: A low-power dual-mode sigma-delta modulator using charge-steering opamps,33rd National Radio Science Conference (NRSC) ,2016, pp. 415-420
10. Y. Wang, et al.: Low-power High-speed Dynamic Comparator Using a New Regenerative Stage, IEEE Electron Devices Solid State Circuits (EDSSC) ,2018, pp. 1-2
11. A. M. Maghraby, et al.: A Low-Noise, Low-Power, Dynamic Latched Comparator Using Cascoded Structure, 2020 12th International Conference on Electrical Engineering (ICEENG), 2020, pp. 335-338
12. Y. B. Ni, et al.: A high speed dynamic comparator with low-power supply voltage, IEEE Solid-State Integrated Circuit (ICSIC) ,2018, pp,1-3