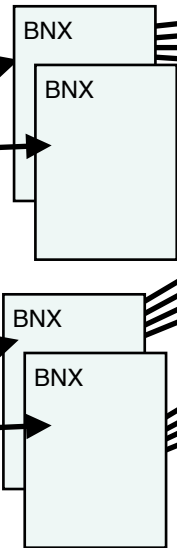


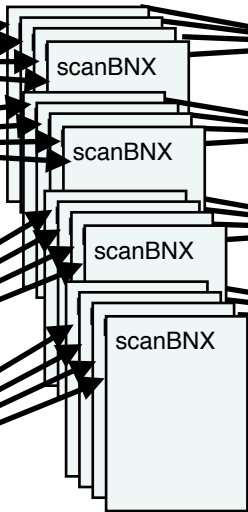
(A) The Irys produces tiff files



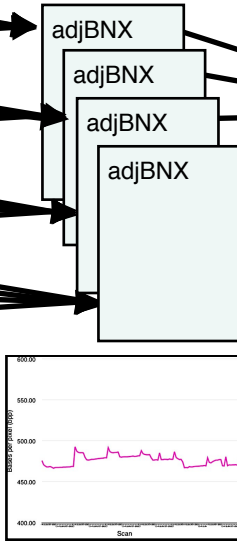
(B) Each chip produces BNX files for two flowcells



(C) Scan BNX adjusted



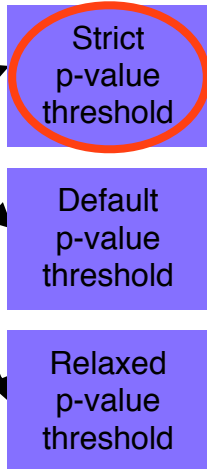
(D) QC graphs for each flowcell



(E) Merge all flowcells in project



(F) First assemblies



(G) Second assemblies

