

A Hybrid FPGA-GPU-based Hardware Accelerator for High Throughput 2D Electrical Impedance Tomography

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Abstract—A high-resolution two-dimensional (2D) electrical impedance tomography (EIT) system requires a larger number of electrodes and a finer mesh than its traditional counterpart. This increases the required number of measurements and, in turn, the amount of computation for the image reconstruction. Given the inverse and ill-posed nature of the EIT systems, they require a high signal-to-noise ratio (SNR) acquisition system as well as a high-precision hardware accelerator platform. In this paper, we present a field programmable gate array (FPGA)-based acquisition system with a tunable single-frequency current source that can reach an acquisition speed of more than 500 and 2400 frames per second (fps) for an excitation signal frequency of 500 kHz using 32 and 16 electrodes, respectively. The data processing and reconstruction are carried out using the most recent embedded Graphical Processing Unit (GPU, Nvidia Jetson Orin) by utilizing multiple Cuda cores to perform parallel high-speed 2D image reconstruction. Five different algorithms, namely linear back projection (LBP), Tikhonov regularization (TK), one-step Gauss Newton (GN), Landweber (LW), and iterative Tikhonov (ITK), were used for investigation. A gain in speed-up of at least 4 times was observed over the traditional implementations on recent general-purpose computers (PCs). Extensive experiments indicate that the proposed system can yield a throughput of more than 2500 fps for a 16-electrode system with around 8192 mesh elements. This paves the way for EIT systems to be potentially used in high-speed imaging applications as well as in 3D EIT applications which involve even larger amount of mesh elements.

Index Terms—Data acquisition, Electrical tomography, Field programmable gate array (FPGA), Graphics processing unit (GPU), Heterogeneous computing, Image reconstruction.

I. INTRODUCTION

2D electrical impedance tomography (EIT) is a non-invasive and non-hazardous imaging technique used to capture the 2D or 3D conductivity profile of a target region by placing an array of electrodes on its 2D or 3D boundary, respectively. It was suggested in several real-life applications, such as in oil and gas fields, where it was deployed in some multi-phase flow meters (MPFMs) for measuring in real time the flow rates of oil, water, and gas produced by each individual well. Most of the existing MPFMs use Venturi meters to measure the total volumetric flow rate of the moving fluid. However, these meters assume that all the phases are homogeneously distributed across the measurement area using an upstream flow conditioner. This, however, requires a cumbersome flow

conditioner, which does not guarantee a homogeneous distribution of individual phases. Having an imaging system such as EIT in MPFM greatly overcomes this limitation as it yields the actual phase distribution. High-speed EIT systems can also be useful to measure the fluid velocity by using, for instance, two rings of electrodes placed at a predefined distance from each other and then computing the cross-correlation of the two images acquired from the two rings. In the medical field, it is used for permanently monitoring, in a safe manner that is not the case with other imaging techniques, a patient's breath and cervical activity by placing several electrodes around the chest and the brain, respectively. A high-speed EIT system can provide significant benefits by improving the accuracy needed to observe these rapid phenomena.

EIT uses AC electrical current signals to excite one pair of electrodes and then measures the voltage response from the other pairs. This process is generally repeated for all the electrode pairs in a sequential manner. For a given N electrode setup, the number of total measurements can be $N(N - 1)$. A forward finite element model (FEM) is required to be built for the region under investigation in order to determine some terms required in the forward and inverse computations such as the Jacobian or sensitivity matrix. The model divides the region into several small sub-regions commonly referred to as mesh elements (E) as shown in Fig. 1, where, $E \gg N$. The reconstruction of the image region requires an inverse approach, and due to the limited number of measurements and non-linear nature of the signal, the problem is both ill-posed and ill-conditioned. This requires various regularization-based approaches with large computations for images, causing high computation complexity that hinders its real-time performance.

Another challenge of EIT systems in comparison to other imaging modalities such as X-ray imaging, gamma-ray imaging, and computed tomography is their relatively poor spatial resolution [1]. While there are several new algorithms being explored for improving the resolution and quality of the reconstructed image [2]–[4], increasing the number of electrodes can be one potential solution. However, this also increases proportionally the number of measurements and, in turn, the computation complexity. This justifies the reason why most EIT systems are limited to 16 electrodes, in most cases, to capture the two-dimensional (2D) cross section of the target medium. For instance, in [5], a 16-electrode system consisting of two rings of 8 electrodes each was presented to capture images of solid particles flowing through a pipeline. The sys-

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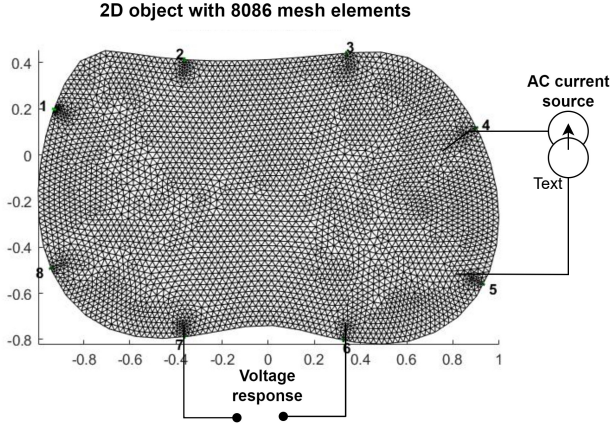


Fig. 1. Principle of an 2D EIT system.

tem acquisition throughput was 100 frames per second (fps), while the image reconstruction was carried out at 67 fps using a general-purpose PC computer. In another recent work in [6], an 8-electrode EIT system targeting robotics applications was developed to localize the position of untethered small scale-robots. It used a 10 kHz excitation signal with a 100 kHz sampling frequency, and 4 cycles per channel were considered for a single channel to increase the SNR, which led to a maximal throughput of only 11 fps for acquisition. Researchers in [7], designed a portable 8-electrode EIT system with a client-server architecture. The server consists of a Xilinx ZYNQ7010 FPGA chip with a built-in dual-core ARM Cortex-A9 microprocessor operating at a maximum clock frequency of 866 MHz. A general-purpose PC was used as a client, which initiated the request to fetch the measurement data. The data acquisition rate of 50 fps and the image reconstruction throughput of up to 40 fps were achieved for a modest 942 pixels per frame using the Generalized Vector Sampled Pattern Matching (GVSPM) algorithm. In [8] a wearable and portable 16-electrode belt was designed. Similar to [7], the processing was done using a general-purpose IBM-compatible PC, while the data was acquired using an Avnet Zedboard with Zynq 7000 (SOC module) at a rate of up to 30 fps. Researchers at the Max Planck Institute for Intelligent Systems designed a 28-electrode EIT system with a current excitation of 24 kHz to yield a 30 fps throughput for predicting the force map of an ERT-based tactile sensor [9]. Another similar system based on Xilinx's FPGA technology was suggested in [10] to yield a throughput of up to 120 fps. While these existing systems are able to capture images at decent frame rates of close to hundreds of frames per second, they are still considered slow for capturing rapid phenomena that occur more frequently in real-world applications. Therefore, there is an urgent requirement for the design of a high-speed EIT system by utilizing the latest of the computing platforms with an optimization approach to carry out the reconstruction in the fastest way possible to increase the speed.

In this paper, a hybrid FPGA and GPU-based heterogeneous platform is proposed to design a high-speed EIT system. The acquisition is carried out using an FPGA based module to

ensure controlled timing execution at clock cycle precision, and a cutting-edge GPU is used for carrying out the image reconstruction. Hence, the most significant contributions of the paper can be listed as follows:

- 1) It suggests a new hardware accelerator for high-speed 2D EIT using the most recent GPU processors for parallel image reconstruction and an FPGA for single-clock-cycle precision of the controlling unit. Most current EIT systems use either general-purpose computers or FPGAs for image reconstruction, which do not yield high throughput.
- 2) A high-speed yet low complexity FPGA based acquisition system based on single current source and its frequency, for operational range of 10KHz to 1 MHz.
- 3) An in-depth assessment of the EIT system in terms of accuracy-throughput and image resolution tradeoffs is disclosed. To the authors' best knowledge, this is the first time that such an assessment is done for 2D EIT on the latest NVIDIA embedded GPU processor, which, as it will be demonstrated, offers great potential for edge-based and portable EIT systems. The suggested system was fully implemented, and all reported experiments were conducted on this platform.

The content of the paper can be summarized as follows: The next section describes the various reconstruction methods and challenges with high-quality 2D EIT systems, followed by the proposed hybrid hardware architecture for very high-speed data acquisition and 2D image reconstruction. Later, experimental results and comparisons with several existing systems are presented, followed by a discussion and conclusion.

II. IMAGE RECONSTRUCTION AND CHALLENGES

The overall throughput of the EIT systems is defined by both the acquisition and the data processing (reconstruction) modules. While there have been multiple solutions to increasing the acquisition speeds, such as multi-frequency or partial measurements or improved hardware, the reconstruction has been mostly limited to utilizing general-purpose PC [11] with some standard library such as EIDORS [12] for carrying out the computation. The computation involves several matrix-based calculations in an iterative or non-iterative way for 2D image reconstruction.

At first, a forward model is prepared from which a sensitivity matrix is derived. This matrix along with the measurement data is then used for reconstruction. Some of the most widely used methods are discussed below:

- 1) Linear back projection (LBP): This is one of the simplest methods that can be used for image reconstruction, and is given as,

$$\sigma = S^T V_i \quad (1)$$

where, σ is the reconstructed image conductivities of size $E \times 1$, S is the sensitivity matrix prepared using the forward model of dimension $M \times E$, and V_i is the voltage measurements ($M \times 1$).

- 2) Tikhonov regularization (TK): It uses a regularization term to solve the inverse problem and is given as,

$$\sigma = (S^T S + \lambda I)^{-1} S^T V_i \quad (2)$$

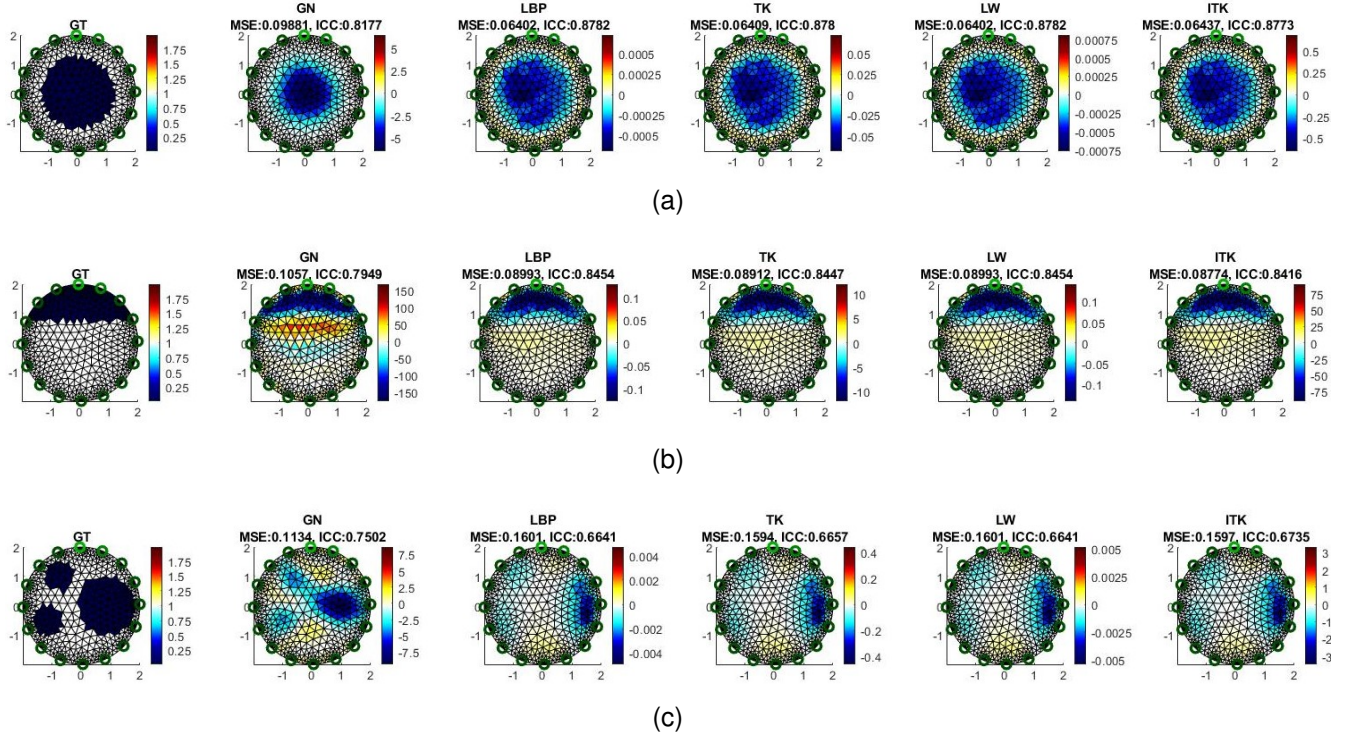


Fig. 2. Reconstructed images under three different scenarios, (a) annular flow of low conductive material, (b) stratified flow, and (c) distributed low conductive material

where, λ is a scalar hyperparameter and I is the identity matrix.

3) One-step Gauss Newton (GN): This is given as,

$$\sigma = (S^T W S + \lambda^2 R)^{-1} S^T W Y \quad (3)$$

where, W is the inverse of the measurement covariance, and considering the measurements to be independent, it is a sparse diagonal matrix of dimension $M \times M$. R is the sparse regularization matrix with dimension of $E \times E$, and Y is the difference of measured potential with a reference signal.

4) Landweber (LW): This is an iterative method to reconstruct the image and is given as,

$$\sigma_{k+1} = \sigma_k - \alpha S^T (S \sigma_k - V_i) \quad (4)$$

where α is a relaxation factor, which determines the rate of convergence, $(S \sigma_k - V_i)$ is the voltage difference in the measured and the estimated value from the forward model during the k^{th} iteration.

5) Iterative Tikhonov (ITK): This is the iterative version of Tikhonov method and is given as,

$$\sigma_{k+1} = \sigma_k - (S^T S + \lambda I)^{-1} S^T (S \sigma_k - V_i) \quad (5)$$

Figure 2 shows the reconstructed image using the above mentioned algorithms for different conductivity distributions. Here, the mean squared error (MSE) given as,

$$MSE = \frac{\sum_{i=1}^E (\sigma_i - \epsilon_i)^2}{E} \quad (6)$$

where, ϵ is the actual conductivities, and the image correlation coefficient (ICC), given as,

$$ICC = \frac{\sum_{i=1}^E (\sigma_i - \bar{\sigma})(\epsilon_i - \bar{\epsilon})}{\sqrt{\sum_{i=1}^E (\sigma_i - \bar{\sigma})^2 \sum_{i=1}^E (\epsilon_i - \bar{\epsilon})^2}} \quad (7)$$

are used to measure the quality of a reconstructed image. The choice of a suitable algorithm is dependent on the application and should be made based on the requirements in terms of quality and processing time. For example, in the annular flow shown in Fig. 2a, LBP, the simplest of the algorithms, performs slightly better than others, while in the distributed case shown in Fig. 2c, GN performs better.

The quality of the final reconstructed image also depends on the number of electrodes and the number of mesh elements. Figure 3 shows the ground truth image, and the reconstructed image quality with different numbers of electrodes in terms of MSE and ICC. Figure 4 shows the reconstructed images using the one-step GN method for different electrode counts. It can be observed that the quality increases with the increase in the number of electrodes. Therefore, for a high quality EIT systems, it is desirable to have a large number of electrodes. Similarly, the number of mesh elements defines the final resolution of the image, and it is again desirable to have a large number of fine mesh elements. Furthermore, iterative methods produce higher-quality images in some cases, as evidenced by several texts and research studies [13]–[16]. Considering all these factors, to improve the quality of the image for high-speed EIT systems, it becomes necessary to carry out the reconstruction computation in an efficient manner to reduce the reconstruction time.

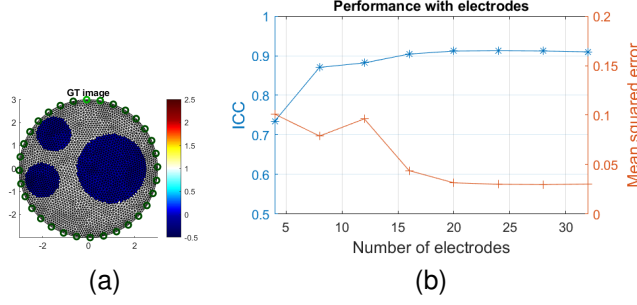


Fig. 3. Performance with different number of electrodes, (a) Ground truth image with non-conductive objective in a conductive medium, (b) Reconstructed image quality in terms of MSE and ICC.

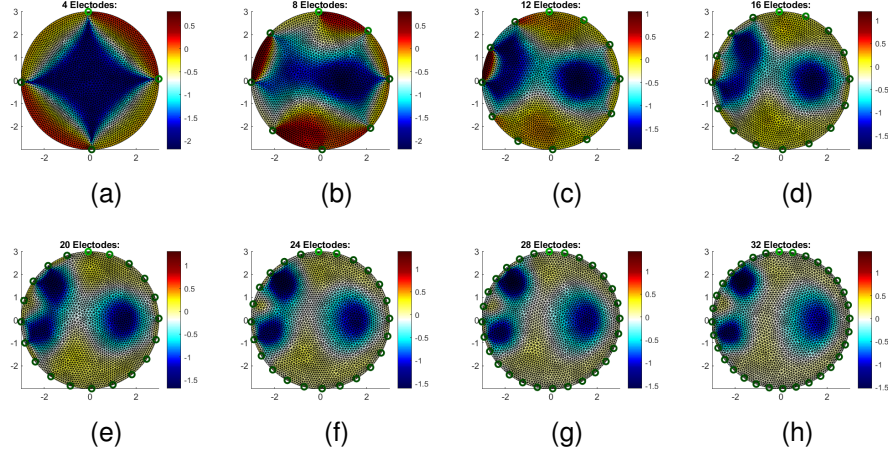


Fig. 4. Reconstructed images with different number of electrodes, (a) 4 electrodes, (b) 8 electrodes, (c) 12 electrodes, (d) 16 electrodes, (e) 20 electrodes, (f) 24 electrodes, (g) 28 electrodes, (h) 32 electrodes.

III. PROPOSED EIT HARDWARE ACCELERATOR

Figure 5 shows the hardware block diagram of the proposed EIT hardware accelerator. The acquisition subsystem comprises mainly a powerful and recent FPGA module based on Altera's Cyclone 5, which is interfaced to a high-speed ADC using SPI (parallel) operating to yield 150 Megasamples per second (MSPS) with a 14-bit resolution. FPGA is a preferred implementation as it offers low power consumption, bit-level operation, flexibility to be dynamically or statically reconfigured, and higher speed and timing control when compared to Von Neumann-like architectures. FPGA controls both the demultiplexer module to select the pair of electrodes to excite with electric current or voltage and the multiplexer module to select the pair of sensing electrodes from which the voltage output is to be captured. Prior to the ADC circuit, a signal conditioning module is used to enhance the SNR of the voltage readings. It consists of a high-reconfigurable gain instrumentation amplifier (IA) featuring high CMRR, high GBWP, and very low thermal noise, followed by a low-pass filter to remove eventual DC noise induced by the offset voltage and current bias of the IA. The ADC unit on the ADC-SOC FPGA board has a transformer coupling, which further helps in reducing the thermal noise. The FPGA subsystem consists of several parallel but synchronized modules to enable high-speed data capture and serial transfer to the GPU board at

a baud rate of up to 12 Mbauds. It also computes the maximal peak voltage corresponding to all channels within a single excitation cycle.

It is worth noting that the suggested hardware accelerator can also be adopted for ECT (Electrical Capacitance Tomography) by only substituting the current source with a voltage source and by considering larger electrodes to form capacitance with reasonably measurable values. Similarly, the accelerator can operate as an electrical magnetic tomography (EMT) system by only substituting the plate electrodes with coils.

A. FPGA-based Acquisition Subsystem

The FPGA-based acquisition subsystem operates at a base clock of 50 MHz, while the ADC module operates at a clock frequency of 150 MHz, which is generated using an internal PLL. A single frame acquisition requires a total of $N(N-1)$ measurements of the signal peak captured after switching channels. The acquisition is performed sequentially, and a GET_MAX module is used to capture the peak, which operates at 150 MHz in synchronization with the ADC data capture module. One full signal cycle (FC) is used to capture the peak amplitude. An external synchronization signal from the main current source is used to trigger this data capture process, which makes this system more flexible. Figure 6

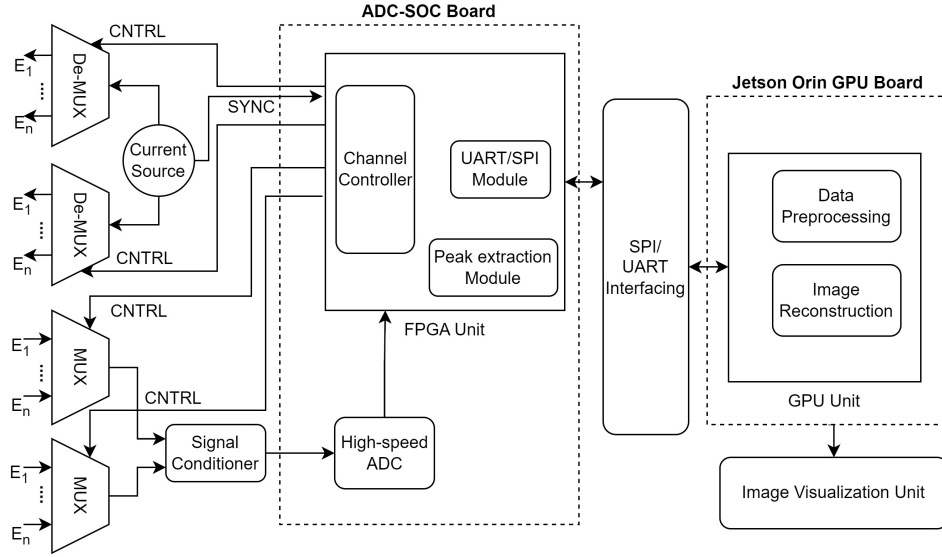


Fig. 5. EIT hardware system.

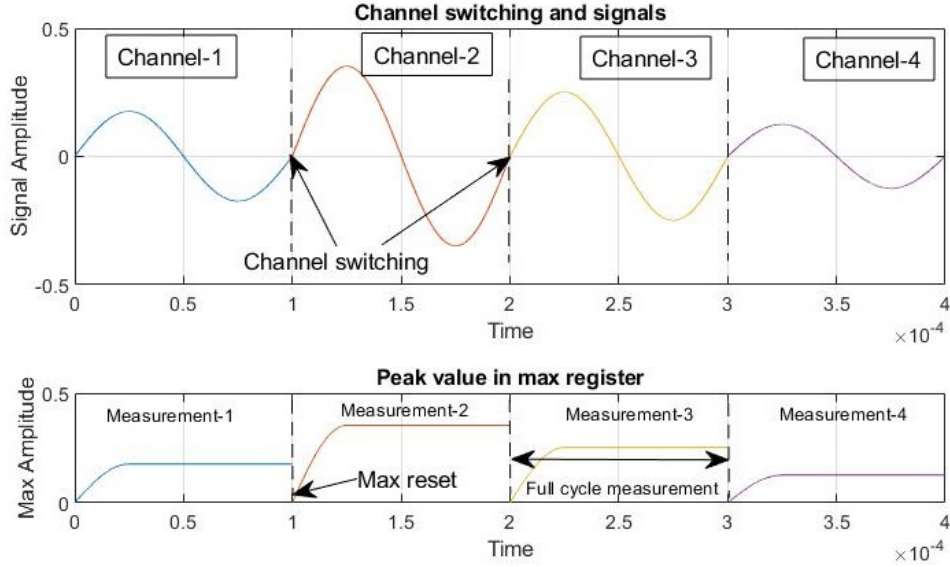


Fig. 6. Proposed acquisition scheme.

shows the proposed acquisition scheme, where channel switching is performed using multiplexers and demultiplexers. The data register of the GET_MAX module contains the peak value of the signal captured over one cycle, which represents one measurement. This register is reset every time before mux/demux switching. The maximum value of this register is used by the communication module to send the data to the GPU for image reconstruction. There is one clock cycle delay between data read and reset to ensure no data loss.

The signal frequency typically used in EIT systems ranges from a few kHz to 1 MHz. Therefore, it is possible to have an online data transfer capability. After each channel selection, the data transfer module initiates the transfer of the captured data for the last channel. As shown in Fig. 6, one full cycle of the signal frequency is used for the peak amplitude

measurement. However, it is possible to further increase the acquisition speed by utilizing only the first half cycle (HC) of the signal, in which case the signal propagation delay of the multiplexers may not be negligible if the source signal frequency is high. Finally, Fig. 7 shows the register transfer level (RTL) view of the FPGA-based modules. The complete system was implemented on an Altera ADC-SOC board, which consists of a Cyclone 5 (5CSEMA4U23C6) device. The system utilized a total of 1682 registers, 702/15,880 (4%) ALMs, 1,245,184/2,764,800 (45%) block memory bits, and one PLL. No DSP blocks were required for this implementation.

Most of the existing acquisition systems employ a sequential data capture method with a single signal frequency. With these systems, the acquisition speeds are limited to tens or hundreds of frames per second. To overcome this, a multi-

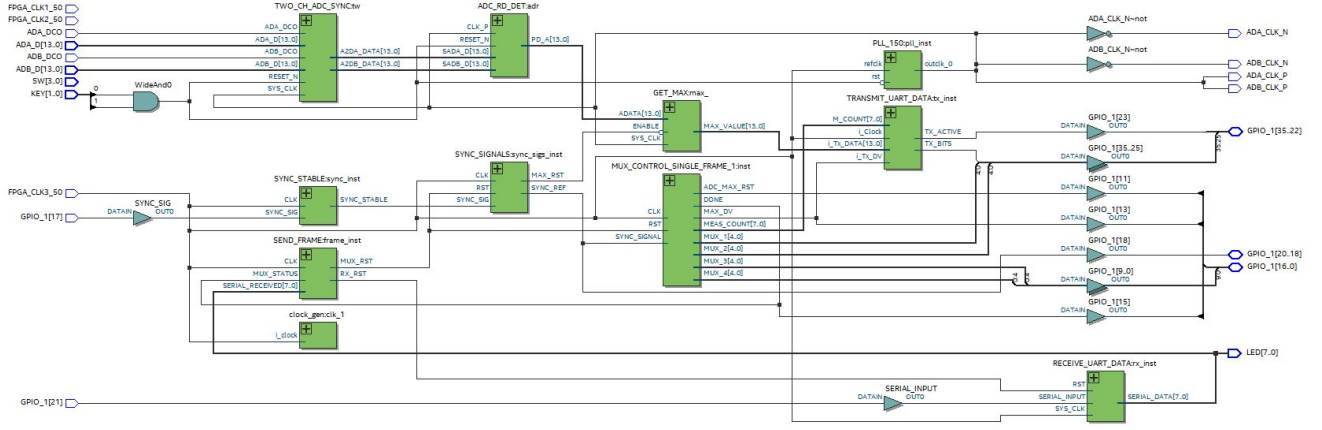


Fig. 7. RTL view of the complete acquisition module.

TABLE I
COMPARISON WITH OTHER EIT ACQUISITION SYSTEMS

Ref.	Elec.	Method	Frame rate
[10] (2017)	16	single frequency (50 KHz)	120 fps
[17] (2021)	16	single frequency (50 KHz)	400 fps
[18] (2017)	32	multi frequency (10 KHz - 1 MHz)	1014 fps
[19] (2020)	16	multi frequency (3.906 kHz-468.7 kHz)	3906 fps
[20] (2019)	16	partial measurement	10000 fps
Proposed	16	External triggered single frequency (10KHz-500 KHz)	FC: 48-2403 fps HC: 96-4806 fps
	32	External triggered single frequency (10KHz-500 KHz)	FC: 10-538 fps HC: 21-1077 fps

frequency excitation-based method was utilized [18], [19]; it allowed significant gains in acquisition speed, up to thousands of frames per second, but at the cost of increased hardware complexity and required more computation and power. A partial measurement was another method that was utilized to increase the frame rate, but at the cost of poor resolution. The authors in [20], used partial imaging and limited measurement to achieve a high frame rate. Only around 10% of the total measurements were carried out for partial imaging. In the proposed approach, the high-speed acquisition speed is designed to be based on the single signal frequency only, with a full measurement carried out in a sequential manner but with low hardware complexity. The transformer-coupled low-noise high-speed ADC enables stable signal characteristics after channel switching, and due to this, it is possible to achieve a high SNR measurement even with one signal cycle. The frame rates achieved are better than the traditional systems while being closely comparable with the multi-frequency systems, with the added advantage of being externally configurable based on the current source signal frequency. Table I shows the comparison of the proposed acquisition system with several recent existing systems.

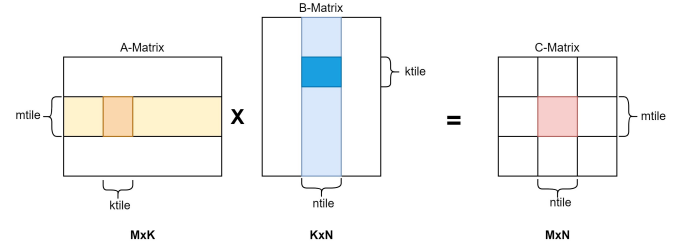


Fig. 8. Tiles based matrix multiplication on GPU.

B. Suggested Image Reconstruction Hardware Accelerator

For computation with a smaller matrix, a general-purpose CPU can be faster than a GPU as long as the matrix can fit into the cache memory. However, as discussed earlier, the size of the matrices involved in the reconstruction increases with the increase in electrodes and mesh elements. Therefore, for a high-quality EIT system, large matrix-based computations are needed. This can be achieved by utilizing the multiple cores of a GPU in parallel. For instance, for matrix multiplication, the output matrix can be partitioned into smaller tiles, which are then processed by multiple thread blocks in parallel. Figure 8 shows the tile-based matrix multiplication of two matrices A and B of dimensions $M \times K$ and $K \times N$, respectively. The output matrix is partitioned into multiple small $mtile \times ntile$ tiles, which are assigned to multiple thread blocks in parallel for execution. Each thread block computes the output by loading the required values from matrices A and B. This operation can also be achieved by stepping through small $ktiling$ steps for very large matrices or GPUs with small cache memory.

In conventional GPU systems, the host (CPU) initiates the program execution on the GPU by first carrying out the data transfer from the host memory to GPU memory, and then the program is executed on the GPU followed by result transfer to the host memory. This type of architecture suffers from memory bandwidth issues, especially when the algorithm requires frequent data access. However, the modern edge GPUs, such as NVIDIA's Jetson Orin, overcome the issue by having an integrated memory architecture for the CPU as well as the GPU. The Jetson Orin is the latest embedded GPU from

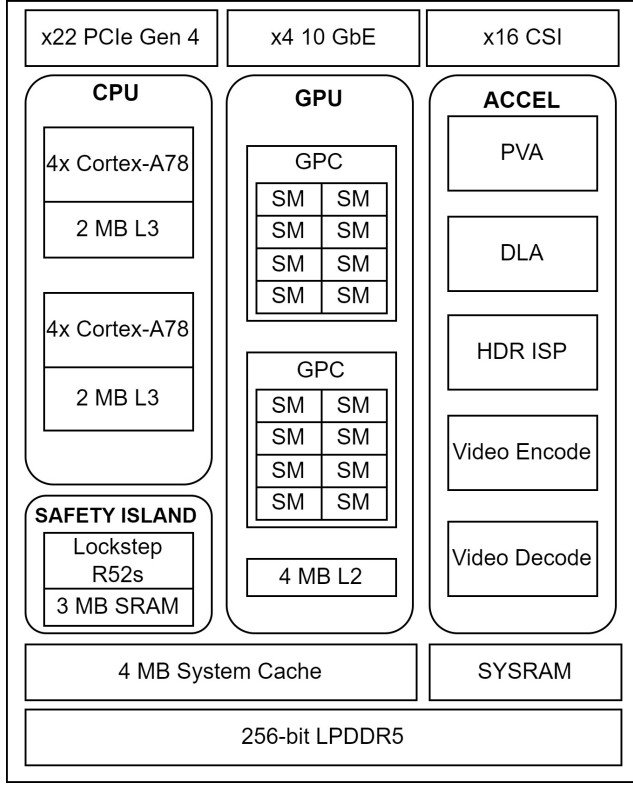


Fig. 9. Nvidia Jetson Orin block diagram.

Nvidia, and it offers around 3.7x and 1.85x more performance for CUDA and CPU compared to its predecessor, the Jeston Xavier [21]. The GPU operates at a maximum frequency of 930 MHz, while the CPU operates at 2.2 GHz. Both the CPU and GPU have access to 32 GB of 256-bit interface, high-speed LPDDR5 memory, supporting a maximum clock speed of 3200 MHz that can transfer data at a speed of 204.8 GB/s. Therefore, the image reconstruction is carried out on this platform using the tile-based approach. Figure 9 shows the block diagram of the embedded GPU. It has 8 ARM CPU cores and 1792 CUDA cores. Nvidia provides CUDA toolkit APIs that can be used to implement optimized reconstruction algorithms by utilizing all the CUDA cores for parallel execution. Several libraries are nowadays available, even in high-level languages such as Python, that can interact with these APIs to have faster execution. NUMBA [22] and CUPY [23] are two such widely used library packages. All the methods discussed in the previous section were implemented on this platform using these libraries for parallel accelerated execution. The edge GPU also provides a dedicated UART/SPI communication capability, which is used for data transfer from the FPGA to the GPU memory. Figure 10 shows the image of the actual hardware setup used for experimentation in this work. The next section presents the experimental results.

IV. EXPERIMENTAL RESULTS

The image reconstruction was implemented for all the methods discussed in section II for CPU as well as GPU execution using the proposed approach for proper comparison.

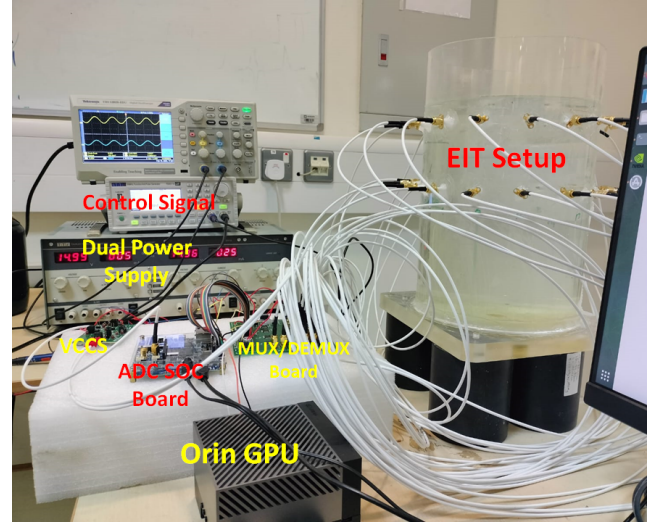


Fig. 10. Actual hardware setup used in the experiment.

TABLE II
RECONSTRUCTION TIME COMPARISON

Method	PC	Edge CPU	Edge GPU	Gain factor (PC/GPU)
LBP	1.5629 ms	0.5247 ms	0.3867 ms	4.0416
TK	1.562 ms	0.3345 ms	0.2505 ms	6.2355
GN	17.288 s	22.795 s	3.3813 s	5.1128
LW (10 Itrs.)	25.6008 ms	32.0696 ms	4.4956 ms	5.6946
ITK (10 Itrs.)	19.1912 ms	9.193 ms	4.2203 ms	4.5474

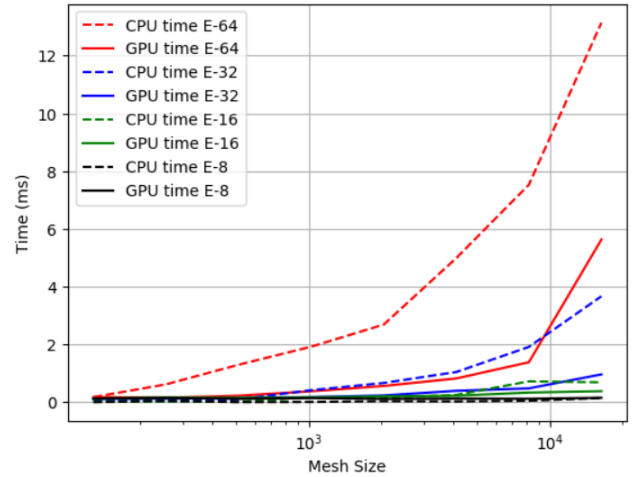


Fig. 11. Execution time with different electrode count and mesh size for LBP algorithm.

Three computing platforms were used: a general purpose PC (64-bit, 4-cores, Intel Core i7-4790S CPU @ 3.20GHz with 256 KB L1, 1MB L2, 8MB L3, and 8GB DDR3 RAM), an Orin CPU (64-bit, 8-cores, ARM Cortex-A78AEv8, 3MB L2, and 6MB L3), and an Orin GPU (32GB, 1792 cores, 4MB L2). The terms such as $(S^T S + \lambda I)^{-1} S^T$, in the case of TK and ITK that involve matrix inversion, do not need to be computed every time. These are computed once, and this leaves only a matrix multiplication for image reconstruction, which further

TABLE III
COMPARISON OF FRAME RATE WITH EXISTING EIT SYSTEMS

Ref.	Elec.	Mesh	Method	Frame rate	Hardware
[7]	8	942	Generalized Vector Sampled Pattern Matching	40 fps	PC
[26]	8	4096	Interframe correlation based	560 fps	Altera Stratix 10 FPGA@ 400-MHz
[24]	8	4096	LBP	3233 fps	Altera Stratix V FPGA,305K LEs
[25]	16	300	Iterative GN	4000 fps	NVIDIA GTX 970,@1.215GHz,4GB DDR5
[27]	16	576	GN(one-step)	0.155 fps	PC (Intel core i5,16GB, @2.3 GHz)
[2]	16	576	EIT-NN, GN, Iterative GN	15 fps, 1000 fps, 0.3676 fps	PC
[28]	16	1024	SALSA	32 fps	PC (Intel corei7, 4GB, @2,2GHz)
[29]	16	4096	LBP	67 fps	PC
Proposed	16	8192	LBP, TK, GN(one-step), LW, ITK	2585 fps, 3992 fps, 0.2957 fps, 222 fps, 236 fps	Nvidia Jetson Orin GPU

helps in improving execution time. Finally, Table II shows the execution time of these reconstruction methods on these three platforms. The CPU implementation of the reconstruction was performed using NUMPY, which exploits the multiple cores of the CPU by using single instruction multiple threads (SIMD) for carrying out large instructions. It can be observed that while the PC has a powerful CPU, it supports a lower number of threads than the ARM CPUs on the Jestson Orin; therefore, the execution was faster on the ARM CPU. CUPY, on the other hand, uses the GPU cores to execute the program. The results are presented considering a 16-electrode EIT setup with 8192 mesh elements. The execution time is evaluated by averaging over 10,000 runs for each reconstruction method. It can be seen that the gain with an embedded GPU is significant, exceeding by at least four times. Figure 11 shows another plot for execution time comparison, LBP-based reconstruction with different numbers of electrodes and mesh counts are shown here. The GPU gain is clearly visible, and it increases as the electrode and mesh counts increase. However, for EIT applications requiring a lower number of electrodes and a lower mesh count, a CPU execution will still be suitable.

Table III shows the comparison of the proposed approach with other existing ET systems. It can be observed that a general-purpose PC is widely used for the reconstruction of the image, with a few implementations utilizing FPGAs or external GPUs. A detailed review of some recent work for image reconstruction can be found in [11]. The reconstruction speed is directly dependent on the number of electrodes and mesh elements. Mostly, the speed was limited to hundreds of frames per second with the PC, but with FPGA-based systems, a frame rate of up to 3233 fps was achieved in [24] using LBP for reconstruction. However, the number of electrodes was only eight, and the mesh count was 4096. The GN method used in [2], [25], does not include the inverse of the measurement covariance W , which removes the limitation of inverse computation for every frame and therefore a higher speed can be observed. However, the number of mesh elements in both cases is still very low (<600). Most of the previous implementations have been limited to 4096 mesh elements or much lower, while with the proposed approach, a frame rate of up to 3992 can be achieved for a 16 electrode setup with as many as 8192 mesh elements. Thus, a memory-integrated GPU-based platform is more suitable for designing next-generation high-speed EIT systems.

V. DISCUSSION

The proposed hardware accelerator for EIT with the combination of an FPGA and GPU-based approach provides high timing control and computing power with flexibility to adapt to different signal frequencies, electrodes, or mesh counts. The high-speed ADC provides support for having a high frame rate. For an ADC with a 14-bit resolution, the total number of bits to be transmitted per frame is $14 * N(N - 1)$. The modern UART protocol on edge GPUs provides a baud rate of up to 12 Mbps [21]. Therefore, considering the two bytes per measurement with one clock separation between packets, the supported speed for a 32 electrode setup can be 646 fps, which is sufficient for a system with a signal frequency of up to 500 kHz that can capture at 538 fps. Both data capture and data transfer can work simultaneously in this case. The data transfer request is initiated by the GPU using a special byte sent over UART. The FPGA starts the data capture and transfer once the start request is made. The overall frame rate of the system is dependent on both the acquisition rate and the reconstruction rate. As discussed previously, the reconstruction time is highly dependent on the type of algorithm and the application requirements. Nevertheless, for the one-step GN method, which is computationally intensive, a full reconstruction was carried out on the edge GPU about 5.1 times faster than the PC for a 16-electrode system with 8192 mesh elements, which is sufficiently large for a 2D system. For other reconstruction methods, such as LBP, that require only matrix multiplication, the reconstruction time can be significantly less. A much higher speed can be achieved when using these methods; for instance, a frame rate of 2585 can be achieved for LBP with 16 electrodes and 8192 mesh elements. In this case, the SPI protocol can be exploited for data transfer. The Orin supports SPI with up to 50 Mbps in slave mode and 65 Mbps in master mode, which means an acquisition speed of more than 3000 fps can be easily supported at higher signal frequencies.

VI. CONCLUSION

The paper presents an FPGA-GPU-based hybrid platform for the design of high-speed EIT systems. Most of the existing systems have used general-purpose PCs for the EIT systems, and this limits the frame rate of the system due to the high computing demand from the reconstruction algorithms.

While some of the previous works have utilized GPUs for reconstruction, they were mostly external GPUs connected to a host PC. This kind of system still suffers from the limitations of the data transfer capabilities between the host memory and the device memory. This paper presents the use of an integrated memory GPU platform for EIT reconstruction methods. The results show that the reconstruction time can be reduced by a factor of 5.1 as compared to a general-purpose PC. The high-speed system can be used in the oil field, as a part of a multi-phase flow meter, or to monitor vessels' contents. It can also be used in medical intensive care units, for instance, to monitor real-time brain activity. In the future, the proposed approach can be easily extended to the design of 3D EIT systems.

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