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Novel high-speed level up-shifter design for improved delay, duty cycle and skew.

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Abstract

High-speed level-up shifters (HSLS) are key components in low-power, high-speed CMOS I/O links. Conventional HSLS designs rely on single-ended to differential converters, which add delay, power, and degrade output duty cycle accuracy. This work introduces a novel HSLS that eliminates the need for explicit conversion by using delay interpolation, improving differential duty cycle centering while reducing power and latency. Additionally, conventional HSLS architectures suffer from single ended duty-cycle distortion and P/N skew. To address this, an auxiliary source follower is proposed to correct these distortions systematically. The combined techniques result in a superior HSLS architecture, demonstrated through PVT and Monte Carlo simulations (1000 samples), with performance compared to a traditional design

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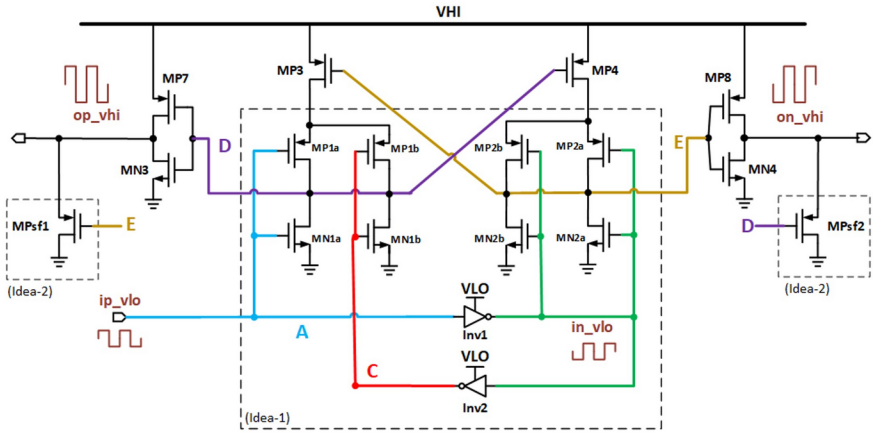
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