

An Improved kT/C noise cancellation Tech-nique with Presampling for SAR ADCs

Yuanfan Gu¹, Kai peng Wang¹, Tiange Yi¹, Xiaoguo Chen², Shiheng Yang¹, and Jiaxin Liu¹

¹University of Electronic Science and Technology of China

²Tsinghua University

August 10, 2024

Abstract

The kT/C cancellation technique can effectively reduce the DAC size for SAR ADCs and thus relax the burden for input drivers and reference buffers. However, the prior kT/C cancellation technique suffers from a hard trade-off between the noise, amplifier bandwidth and linearity. In this work, an improved kT/C noise cancellation technique is proposed to break the trade-off. It uses presampling to hold the input signal unchanged during the noise cancelling phase, leading to significantly relaxed requirements on the bandwidth and linearity of the amplifier. The proposed technique is verified in a 14-bit 200MS/s SAR ADC with the DAC size of 128 fF. Simulation results show that this work achieves 75.6 dB SNDR and consumes 1.56 mW power.

An Improved kT/C noise cancellation Technique with Presampling for SAR ADCs

Yuanfan Gu, Kaipeng Wang, Tiange Yi, Xiaoguo Chen,
Shiheng Yang, Jiaxin Liu

School of Integrated Circuit Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China

E-mail: liujiaxin@uestc.edu.cn

The kT/C cancellation technique can effectively reduce the DAC size for SAR ADCs and thus relax the burden for input drivers and reference buffers. However, the prior kT/C cancellation technique suffers from a hard trade-off between the noise, amplifier bandwidth and linearity. In this work, an improved kT/C noise cancellation technique is proposed to break the trade-off. It uses presampling to hold the input signal unchanged during the noise cancelling phase, leading to significantly relaxed requirements on the bandwidth and linearity of the amplifier. The proposed technique is verified in a 14-bit 200MS/s SAR ADC with the DAC size of 128 fF. Simulation results show that this work achieves 75.6 dB SNDR and consumes 1.56 mW power.

Introduction: The SAR is a popular ADC architecture with simple structure and low power. Aside from the ADC core, in practical applications, a SAR ADC often requires the front-end input driver and reference buffer, as shown in Fig. 1. However, limited by the sampling kT/C noise, the input capacitor of a SAR ADC has to be large to achieve high resolution. This makes it costly to design the input driver and reference buffer [1,2]. The kT/C cancellation technique can effectively reduce the DAC size for SAR ADCs, and thus relax the burden for input drivers and reference buffers [3,4]. However, the prior kT/C cancellation technique suffers from a hard trade-off between the noise, amplifier bandwidth and linearity, which is particularly serious in

high-speed applications with high-frequency input signal. In this work, we propose an improved kT/C noise cancellation technique to break the trade-off.

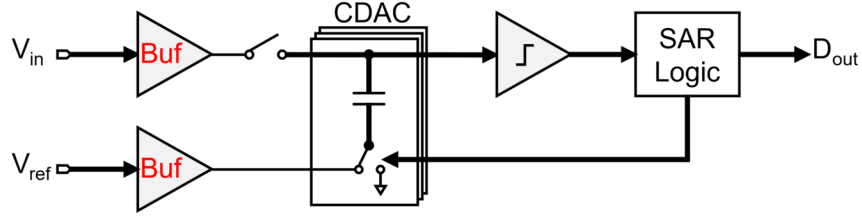


Fig.1 SAR ADC with input driver and reference buffer

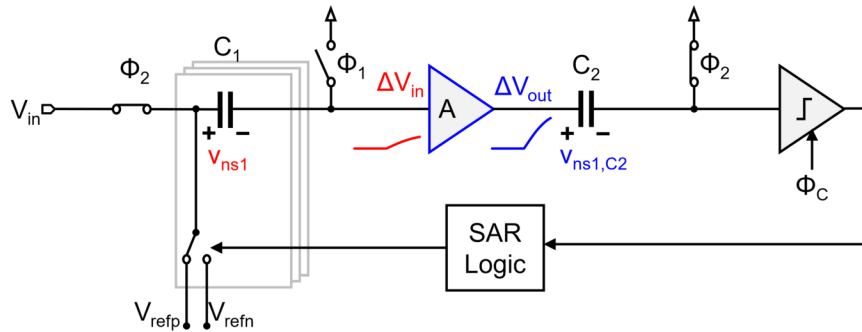
Prior kT/C noise cancellation technique: The kT/C noise cancellation technique originates from the classic output series offset cancellation [5,6]. In [3], it is extended to a switched-capacitor amplifier which realizes the sampling noise reduction in an auto-zero manner. In [4], this technique is used in a SAR ADC. Comparing to [3], it reuses the SAR feedback to close the loop and only requires an open-loop amplifier. The SAR ADC with kT/C noise cancellation [4] is shown in Fig. 2. The sampling operation is divided into two phases, Φ_1 sampling (from t_0 to t_1) and Φ_2 sampling (from t_1 to t_2). During Φ_1 sampling, the input signal is tracked on the DAC C_1 , together with the thermal noise from sampling switches. After Φ_1 sampling, the sampling noise is frozen on C_1 . During the Φ_2 sampling phase, it is amplified and stored on C_2 through the amplifier. In this manner, the sampling kT/C_1 noise is cancelled at the right side of C_2 . Considering the limited bandwidth of amplifier, the kT/C_1 noise cannot be eliminated completely. The noise residue can be expressed as

$$\overline{v_{ns1,res}^2} = kT/C_1 \bullet e^{-2\Delta t/\tau}$$

where Δt is the time duration of Φ_2 sampling, τ is the time constant at the output of amplifier.

To reduce noise, one way is to increase Δt , but this can degrade the linearity of amplifier and even cause saturation because the input signal change during Δt is also amplified. To ensure linearity, the signal change at the amplifier input must be small. As a result, the input signal frequency is limited. Another way is to reduce the time constant τ by increasing amplifier bandwidth, but this is at the cost of increased power. Even if the power budget is sufficient, the bandwidth improvement will be eventually prevented by input transistor size of the amplifier. This is because the large input capacitance of amplifier exaggerates the ADC input-referred noise.

As analyzed above, for the ADCs with kT/C noise cancellation, the signal bandwidth is limited by the trade off between noise, amplifier bandwidth and linearity. The root cause of this issue is that the amplifier has to deal with the input signal change during Φ_2 sampling phase.



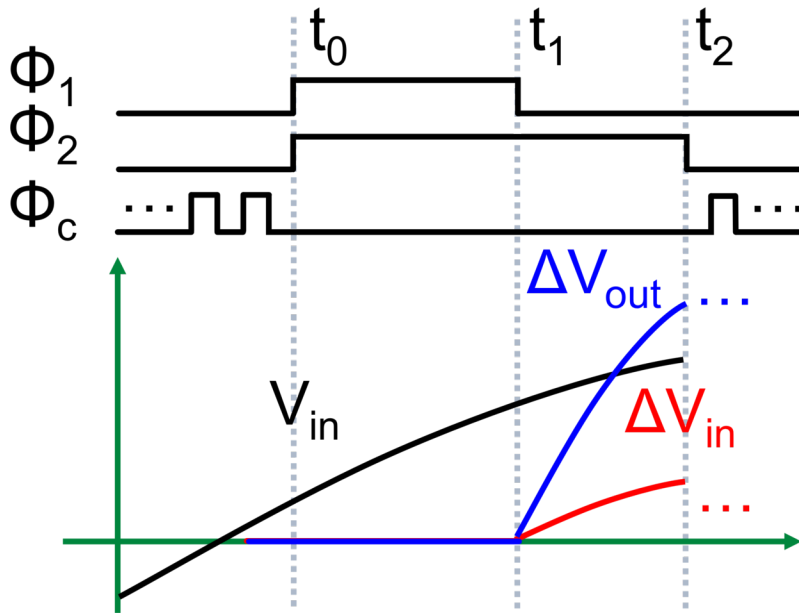
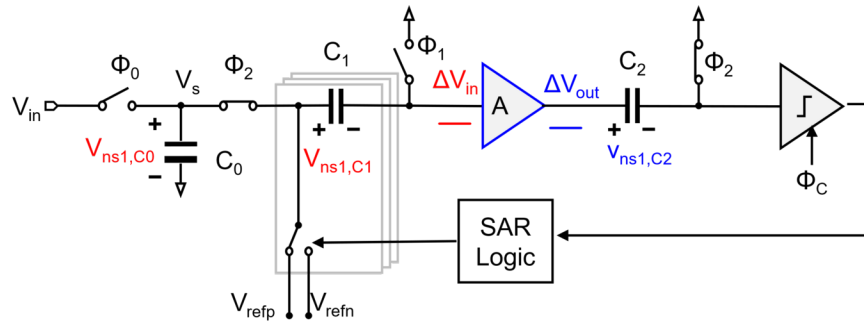


Fig.2 Previous SAR ADC with kT/C noise cancellation

Proposed kT/C noise cancellation SAR ADC with presampling: To break the trade-off, this work proposes an improved kT/C noise cancellation technique with presampling [7]. On top of Fig. 2, an additional switch-capacitor pair, Φ_0 - C_0 , is introduced. C_0 acts as a presampling capacitor, which samples the input signal and holds it during the Φ_2 sampling phase.



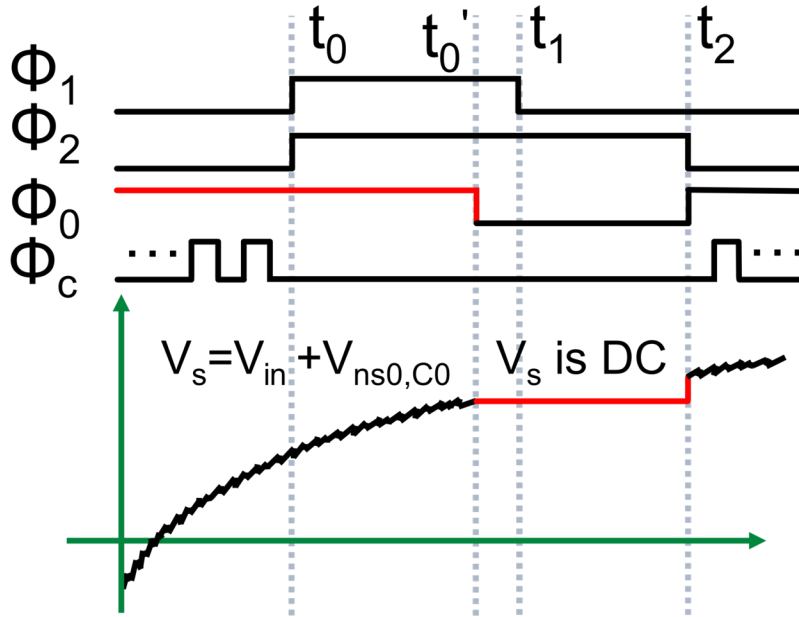


Fig.3 Proposed kT/C cancellation SAR ADC with presampling

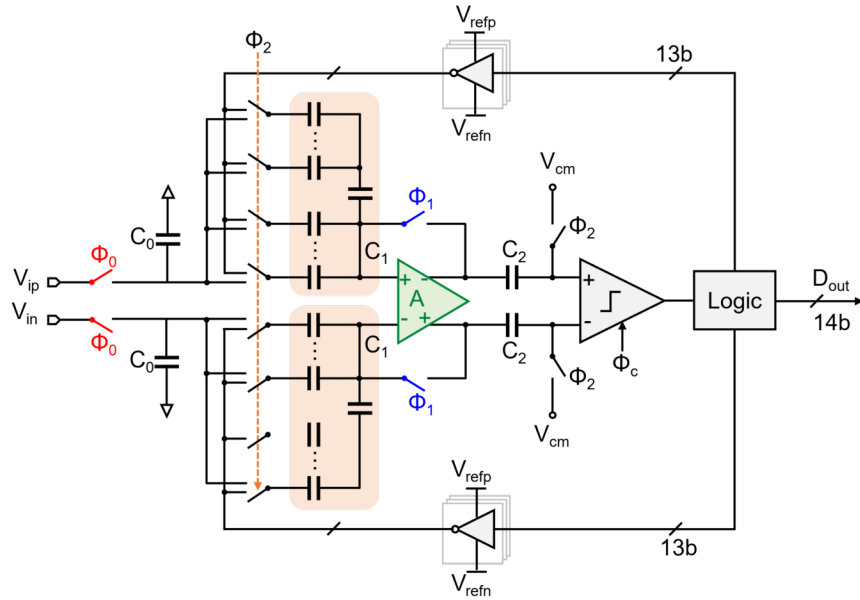
The detailed operation of the proposed kT/C cancellation technique is illustrated in the following:

1. Φ_0 sampling: during Φ_0 is high, the input signal is tracked on C_0 .
2. Φ_1 sampling: at the final stage of Φ_0 sampling, Φ_1 turns on and the input signal is also tracked on C_1 . Then, Φ_0 and Φ_1 turns off in sequence, and the input signal is sampled on C_0 and C_1 .
3. Φ_2 sampling: during t_1 to t_2 , the kT/C_1 noise is amplified and stored on C_2 , which is same as that in [4]. The difference is that there is no input signal change but only the sampled noise at the input of amplifier, because the input signal at the bottom plate of C_1 is hold constantly by C_0 . This eliminates the issues of amplifier saturation and nonlinearity existing in [4]. Therefore, the relatively long Δt and large amplifier gain can be used to suppress the kT/C_1 noise and amplifier noise, respectively.

Comparing to [4], the additional C_0 sampling operation and the kT/C_0 noise are introduced. Since the C_0 sampling noise is not cancelled, a large-size kT/C determined C_0 capacitor is required. Nevertheless, the reason abilities and merits of the proposed technique lies in the following aspects:

1. Although a large C_0 is required, a long C_0 sampling time can be allocated to relax the burden of input driver. As shown in Fig. 3, all the time expect Δt can be used for C_0 sampling.
2. As with [4], the kT/C_1 noise is canceled and thus small DAC can be used to reduce the load for reference buffer.
3. Comparing to [4], this technique suffers no amplifier nonlinear issues, and thus the long Δt and large amplifier gain can be used. This further reduces the kT/C_1 noise and amplifier noise, and also relaxes the requirement on amplifier bandwidth.

Circuit Implementation and Simulation results: A14-bit SAR ADC with the proposed kT/C noise cancellation is designed in a 28nm CMOS process. As shown in Fig. 4, C_0 is 2.8 pF and DAC C_1 is 128 fF. The gain of the amplifier is about 10. The time duration of Δt is 25% of an entire ADC cycle. In comparison, the amplifier gain is 6 and Δt is 2.5% of an ADC cycle in [4]. The increased Δt can relax the amplifier bandwidth requirement.



$$F_s = 200 \text{ MHz}$$

$$C_1 = 128 \text{ fF}$$

$$C_2 = 350 \text{ fF}$$

$$C_0 = 2.8 \text{ pF}$$

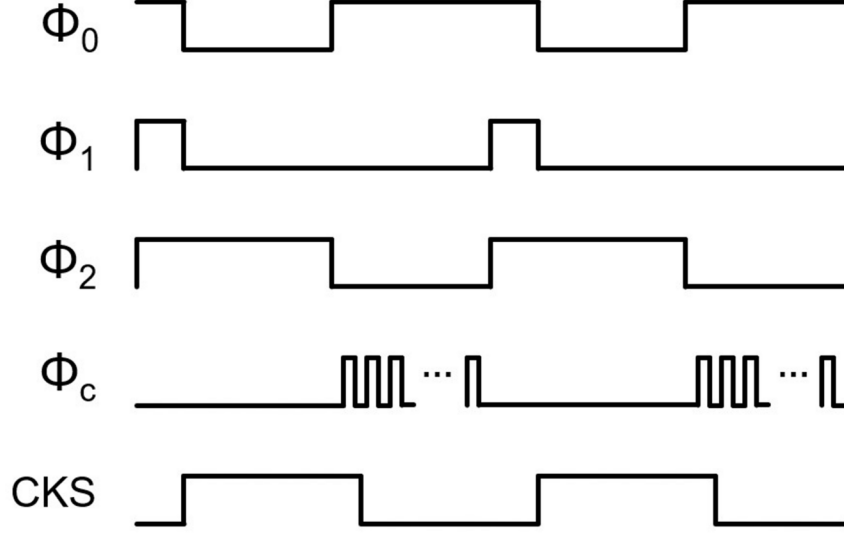


Fig.4 Circuit implementation of the proposed SAR ADC.

Fig. 5 shows the simulated output spectrum. Operating under 1 V supply and 200 MHz sampling rate, the simulated SNDR is 75.6 dB with a 98 MHz input signal. The total power consumption is 1.56mW. This leads to a superior Schreier Figure of Merit (FoMs) of 183.7 dB. The noise and power breakdown are provided in Fig. 6. It shows that 41% of the total power is consumed by the amplifier, 12% by the DAC, 40% by digital circuits and 7% by others. The total noise is 13.7nV_{rms}, with 40% from the amplifier, 23% from kT/C₀ noise, 16% from kT/C₁ noise, 9% from quantization noise and 12% from others.

Hosted file

image17.emf available at <https://authorea.com/users/813439/articles/1214823-an-improved-kt-c-noise-cancellation-tech-nique-with-presampling-for-sar-adcs>

Fig.5 Simulated spectrum.

Fig.6 Noise and power breakdown.

- (a)
- (b)

Fig.7 Simulation results of the sampling circuits in (a) traditional SAR ADC and (b) proposed SAR ADC

Fig. 7 compares the simulated voltage and current waveforms of the sampling circuits in a conventional SAR ADC and the proposed one. For a conventional SAR ADC, in order to leave as much as time to SAR conversion, typically the tracking phase occupies a small portion of an entire ADC cycle. As shown in Fig. 7(a), 13% of an entire ADC cycle is used for tracking. For a near-Nyquist input signal, the maximum input signal change (ΔV_{\max}) on the sampling capacitor is as high as 990 mV and the peak current (ΔI_{\max}) drawn from the input buffer is 44.3 mA. In contrast, for the proposed ADC, the most of an ADC cycle can be allocated for tracking. As shown in Fig. 7(b), 87% of an entire ADC cycle is used for tracking, leading to a short time of disconnection between the input driver and the sampling capacitor. This makes the proposed ADC close to a continuous-time one. Comparing to Fig. 7(a), the maximum input signal change (ΔV_{\max}) on the sampling capacitor and the peak current (ΔI_{\max}) are significantly reduced to 256.3 mV and 15.1 mA, respectively. This verifies that the long tracking time can relax the requirement on the driving capability of input buffer.

Conclusion: This work proposes an improved kT/C noise cancellation technique with presampling for SAR ADCs. Comparing to the previous works [4], the proposed technique effectively addresses the nonlinear issues and relaxes the bandwidth requirement of the amplifier, leading to the improved accuracy and reduced power. Comparing to the conventional SAR ADCs, it greatly increases the tracking time and reduces the DAC size, leading to relaxed burden for the input drivers and reference buffers.

Author Contributions: **Yuanfan Gu** : Data curation; Formal analysis; Validation; Visualization; Methodology; Writing—original draft ; Writing—review & editing. **Kaipeng Wang** : Formal analysis; Methodology; Validation; Writing—original draft; Writing—review & editing. **Tiange Yi** : Formal analysis; Validation; Visualization; Writing—review & editing. **Xiaoguo Chen** : Formal analysis; Validation; Visualization; Writing—review & editing. **Shiheng Yang** : Formal analysis; Funding acquisition; Methodology. **Jiaxin Liu** : Conceptualization; Funding acquisition; Project administration; Resources; Supervision; Writing—review & editing.

Acknowledgments: This work was supported by NSFC under Grant 62174023.

Conflict of interest statement: The authors do not have a conflict of interest to disclose.

Data availability statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

1. C.-C. Liu, C.-H. Kuo, and Y.-Z. Lin, “A 10 bit 320 MS/s low-cost SARADC for IEEE 802.11ac applications in 20 nm CMOS,” *IEEE J. Solid-State Circuits* , vol. 50, no. 11, pp. 2645–2654, Nov. 2015.
2. W.-H. Tseng, W.-L. Lee, C.-Y. Huang, and P.-C. Chiu, “A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for digitally-assisted wireless transmitters,” *IEEE J. Solid-State Circuits* , vol. 51, no. 10, pp. 2222–2231, Oct. 2016.
3. R. Kapusta, H. Zhu, and C. Lyden, “Sampling circuits that break the kT/C thermal noise limit,” *IEEE J. Solid-State Circuits* , vol. 49, no. 8, pp. 1694–1701, Aug. 2014.
4. J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, “A 13-bit 0.005-mm² 40-MS/s SAR ADC with KT/C noise cancellation,” *IEEE J. Solid-State Circuits* , vol. 55, no. 12, pp. 3260–3270, Dec. 2020.
5. R. Poujois, B. Baylac, D. Barbier, and J. Ittel, “Low-level MOS transistor amplifier using storage techniques,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 16, Feb. 1973, pp. 152–153.
6. B. Razavi and B. A. Wooley, “Design techniques for high-speed, high resolution comparators,” *IEEE J. Solid-State Circuits* , vol. 27, no. 12, pp. 1916–1926, Dec. 1992.
7. J. Liu, et al. ”A method for effective sampling noise cancellation in SAR ADC applications.” Chinese Patent CN202311327504.X, pub. October 13, 2023.