Large-area MoO x /c-Si heterojunction solar cells with a ICO/Ag back reflector

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Abstract

Compound/silicon heterojunction (SCH) solar cells have been widely studied due to the low parasitic absorption of the window layer, high short-circuit current, and simple preparation process. So far, most reported SCH solar cells are small-area devices. By depositing MoO$_x$ hole transport layer using hot-wire oxidation-sublimation deposition technique and employing a front-contact back-junction cell architecture, the large-area SCH solar cells are successfully fabricated on M6 (166 mm) n-type silicon wafers. Indium cerium oxide (ICO) film with the optimal thickness of about 110 nm is inserted between MoO$_x$ and Ag. The ICO/Ag stack functions well as a back reflector and is beneficial for increasing the short-circuit current density, reducing the contact resistance, and improving the device stability. A power conversion efficiency of 21.59% is achieved on the champion SCH solar cell with the device area of 274.15 cm^2.

1 Introduction

Silicon solar cells with passivation contact structures utilize hydrogenated amorphous silicon (a-Si:H) or silicon oxide (SiO$_x$) as a highly effective passivation layer[1,2]. This layer is inserted between the crystalline silicon (c-Si) wafer and the carrier transport layer, resulting in drastically reduced interface recombination losses and higher efficiency when compared to PERC (Passivated Emitter and Rear Cell) solar cell. An exemplary type of solar cells using passivation contacts is the silicon heterojunction (SHJ) solar cell, which is known for its high conversion efficiency, simple preparation process and low process temperature. Recently, the power conversion efficiency (PCE) of SHJ solar cell has reached 26.8%[3]. However, the short-circuit current density (J$_{sc}$) of SHJ solar cell tends to be lower than that of PERC cell, which is mostly attributable to the parasitic absorptions of intrinsic a-Si:H (a-Si:H(i)), highly-doped nano-crystalline silicon (nc-Si:H), and transparent conductive oxides (TCO) layer[4,5]. Compared to the passivation intrinsic a-Si:H layer, the parasitic absorption loss induced by the highly-doped nc-Si:H layer is more pronounced, as a certain thickness is required to form an effective built-in potential. In addition, highly-doped nc-Si:H also faces problems such as Auger recombination loss and complex doping techniques using toxic gases.

In order to replace highly-doped nc-Si:H, some dopant-free passivation contact structures have been explored. Compound semiconductors that feature a wide bandgap were used as the carrier transport layer (contact layer) in creating a silicon/compound heterojunction (SCH) solar cell with a c-Si wafer. Theoretically, it has the potential to mitigate energy loss associated with heavy doping, such as Auger recombination, bandgap narrowing, and free carrier absorption[6,7]. Furthermore, the range of work function in compound semiconductors is broader compared to that of doped a-Si:H or nc-Si:H. This characteristic is advantageous in designing and producing devices with higher built-in potentials in principle.

Many oxides and fluorides have been adopted as carrier transport layers. High work function transition metal oxides (TMO), such as MoO_x[8,9], WO_x[10], and V_2O_x[11], are utilized as hole transport layers (HTL) in SCH solar cells. The ones with low work function, such as SnO_2[12], TiO_2[13,14] and LiF[15,16], are used as electron transport layers (ETL). These ETL and HTL compounds can be prepared using some simple techniques, such as thermal evaporation, atomic layer deposition (ALD)[17], electron beam evaporation[18], and spin-coating[19], which have the potential for low-cost compared to plasma enhance chemical vapor deposition (PECVD) commonly used for a-Si:H and nc-Si:H.

Nowadays, SHJ solar cells are mostly based on n-type c-Si wafers and commonly use a front-contact back-junction structure, where n-type nc-Si:H (nc-Si:H(n^+)) layer and p-type a-Si:H (or nc-Si:H) emitter are respectively located on the front and rear side of the cell. The main reason for adopting this structure is that p-type doping of a-Si:H or nc-Si:H has lower efficiency than n-type doping, thus requiring a larger thickness, which leads to more severe parasitic absorption when located on front side of the cell. Therefore, finding new emitter materials with higher transmittance and larger work function to replace p-type a-Si:H or nc-Si:H is more urgent compared to replacing n-type nc-Si:H. MoO_x with a wide bandgap and high work function has been considered the most probable alternative to p-type a-Si:H or nc-Si:H and the MoO_x/c-Si(n) SCH solar cells have received more and more attention [8,9,20]. A PCE of 23.85% has been achieved by Cao and Paul Procel et al. recently[21].

However, the thermal stability of MoO_x/c-Si(n) SCH solar cells is an important issue and it was found that the device performance decreases significantly when annealed above 130 °C[8, 22]. The device degradation could mostly be attributed to the formation of a SiO_x barrier layer at the interface between MoO_x and a-Si:H[14,23,24]. The large area metallization process (screen printing Ag grid) commonly used in SHJ solar cells is not suitable for SCH solar cells, since a solidification temperature of about 200 °C is required. The metal electrode preparation techniques reported in the literature for the SCH solar cells are mainly electroplating[8] or thermal evaporation [14]. Up to now, limited by the metallization process, all the reported MoO_x/c-Si(n) SCH solar cells, no matter front-junction or back-junction, are small-area devices. Besides the metallization process, deposition of MoO_x film is also an important factor hindering the preparation of large-area SCH solar cell. So far, the MoO_x HTL in most of the reported high-efficiency SCH solar cells[20,21] was prepared using thermal evaporation which is not conducive for continuous deposition of uniform large-area films. Exploring large-area SCH solar cell processes is of great significance for future mass production.

In this paper, studies on large-area MoO_x/c-Si(n) SCH solar cells featuring a front-contact back-junction architecture were conducted. Large-area MoO_x films were deposited using hot-wire oxidation-sublimation deposition (HWOSD) technique[25]. By optimizing the device fabrication process flow including screen printing of the silver grids, the MoO_x layer can avoid suffering from high-temperature process. By using ICO/Ag as the back reflector, a power conversion efficiency (PCE) of 21.59% was achieved on the champion SCH solar cell with the size of 274.15 cm^2 (M6).

2 Experimental details

2.1 Fabrication of SCH and SHJ solar cells

N-type (100) oriented Czochralski (CZ) silicon wafers with a thickness of 170 μm and a resistivity of 3 Ωcm were used as the substrates. After alkaline texturing, they were cleaned according to the standard RCA procedures. After cleaning, a 7 nm a-Si:H(i) passivation layer was deposited on both sides of the substrates using plasma enhanced chemical vapor deposition (PECVD). After that, a n-type nc-Si:H layer was deposited on the front of the solar cells using PECVD. An indium cerium oxide (ICO) layer was then deposited on the nc-Si:H(n^+) layer using reactive plasma deposition (RPD). Ag grids were screen printed on the front side and the semi-finished solar cells were annealed at 200 °C for 10 min. Next, a 10 nm MoO_x film was deposited on the rear side using HWOSD and then an ICO film was deposited on the MoO_x layer by RPD. At last, silver electrode was thermal evaporated on the whole rear side to finish the fabrication of the SCH solar cells. It should be pointed out that it is critical to carry out the screen printing process before the MoO_x deposition, otherwise the performance of the SCH solar cells will be significantly reduced. The conventional

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SHJ solar cells were fabricated for a reference. Except for the replacement of the MoO_x layer by a 15 nm p-type amorphous silicon (a-Si:H(p^+)) layer, other processes and parameters are the same as that of the SCH solar cells. The photographs and the structural schematic diagram of the MoO_x/c-Si(n) SCH solar cell and the process flows of the SCH and SHJ solar cells are shown in Figure 1.

2.2 Characterization

External quantum efficiency (EQE) of the SCH solar cells was tested with a quantum efficiency test system (SCS600-XT). Contact resistivity (ρ_c) of the devices was obtained using Keithley 2400 source meter. Light J-V characteristics of the large-area solar cells were calibrated by solar cell sorting machine (DG100) under AM1.5 (100 mW/cm^2, 25 °C) illumination.

3 Results and discussion

(a)

(b)
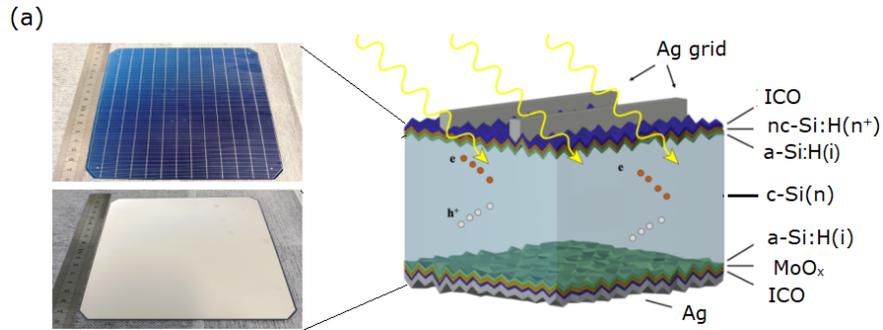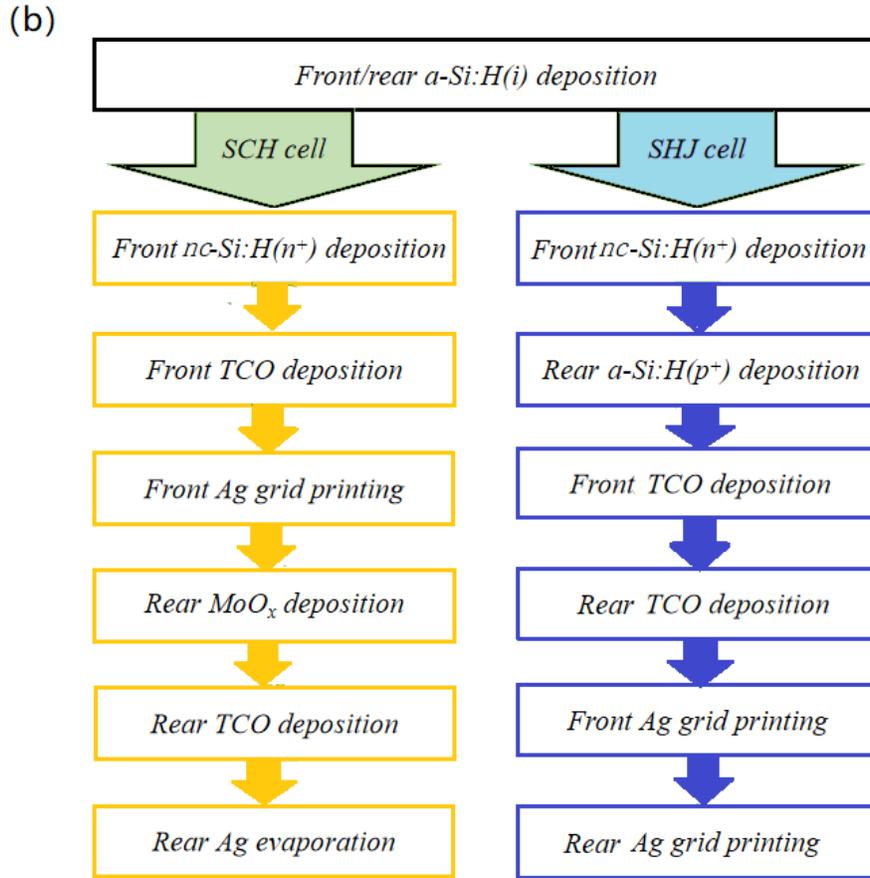
Figure 1 (a) Photographs and structural schematic diagram of a full size (274.15 cm^2) MoO$_x$/c-Si(n) SCH solar cell with front-contact back-junction structure and with an ICO/Ag back reflector. (b) Process flows of the SCH solar cells and SHJ solar cells.

3.1 Effect of ICO/Ag back reflector for SCH solar cell

For most reported SCH solar cells with the carrier transport layer on the back side, the metal electrode was usually deposited directly on the carrier transport layer [26,27]. Although the process is relatively simple, the parasitic absorption of the metal electrode often leads to reductions in the quantum efficiency and J$_{sc}$. Indium cerium oxide (ICO), recently widely used in the SHJ solar cells as the TCO layer, shows excellent optoelectronic properties such as high mobility, high transmittance, and low free carrier absorption[28,29,30]. Here, besides serving as the top transparent electrode, ICO film is inserted between the MoO$_x$ layer and the back Ag electrode in the SCH solar cells as shown in Figure 1 (a). The ICO/Ag combination on the rear of the SCH solar cells was expected to serve as a back reflector.

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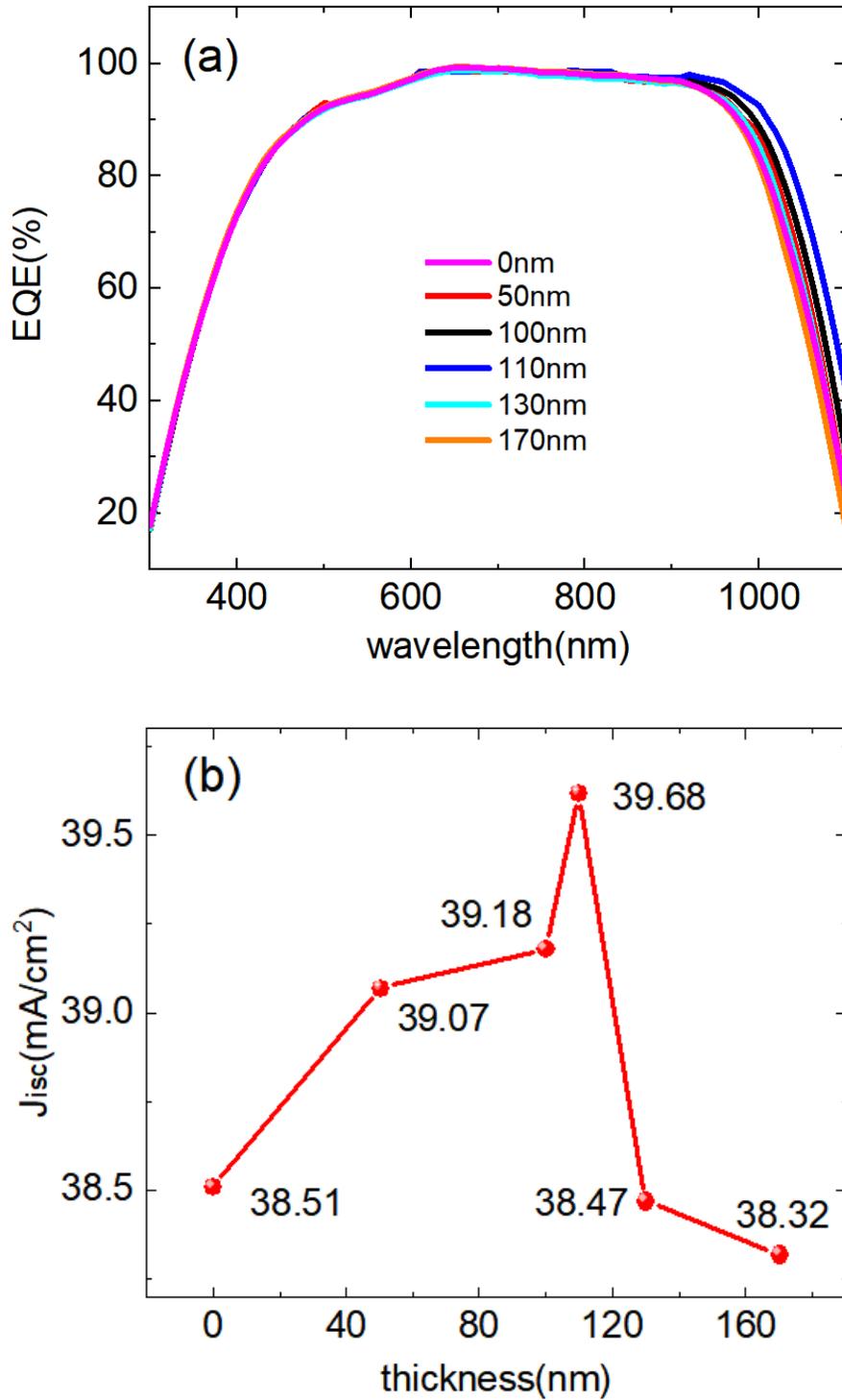
Figure 2 EQE (a) and integrated current J_{isc} (b) of the SCH solar cells with ICO layer of different thickness.

The EQE and integration short-circuit current density (J_{isc}) for the SCH solar cells with back ICO films of varying thickness are depicted in Fig. 2 (a) and (b), respectively. The EQE curves almost overlap in the short wavelength range due to the same front structure. However, the quantum efficiency of long wavelength

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increases first and then decreases with increasing of the back ICO thickness. The back ICO thickness corresponding to the highest EQE is about 110 nm and the corresponding J_{isc} is 39.68 mA/cm^2. As a comparison, J_{isc} for the SCH solar cell without back ICO is 38.51 mA/cm^2. The significant improvements in long wavelength response and J_{isc} by adding the back ICO layer with a suitable thickness of 110 nm indicate that the ICO/Ag combination functions well as a back reflector.

3.2 Contact resistance of a-Si:H(i)/MoO$_x$/ICO/Ag stack

The contact resistance related to the carrier selection transport layer has a significant impact on carrier collection efficiency and solar cell performance. Therefore, investigation of contact resistances of the SCH solar cells, especially the MoO$_x$ HTL side (back side here), is imperative. The main methods for contact resistance measurement include the rectangular transmission line method (TLM)[31], the Cox and Strack method (CSM)[32], and the extended CSM (ECSM)[33]. The electrode structure for CSM and ECSM are the same and it is employed here for contact resistance measurement as shown in Fig. 3 (a). The a-Si:H(i), a-Si:H(p$^+$), TCO and Ag electrodes were deposited successively on the rear side of a p-type silicon wafer to form an ohmic contact. Front side of the p-type silicon wafer was deposited with a-Si:H(i), MoO$_x$, TCO, and Ag in sequence with a metal mask. The purpose of using p-type Si wafer is to reduce the junction effect.

The I-V curves corresponding to c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag contacts with different electrode diameters are plotted in Fig. 3(b). The obvious rectification characteristic indicates that ohmic contacts are not formed. The CSM method is not appropriate for the device featuring junction resistance. Therefore, the ECSM method which can eliminate the impact of rectification effect is used to analyze the contact resistance of the c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag stacks.

(b)
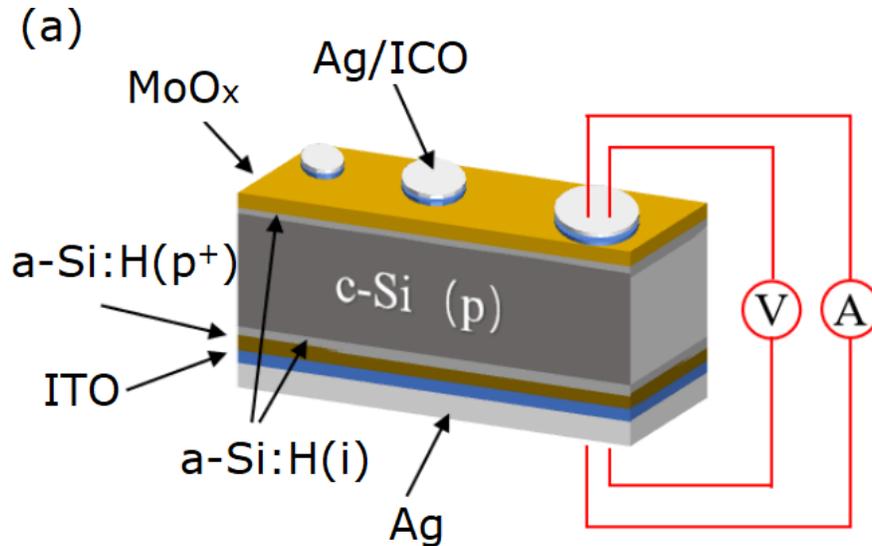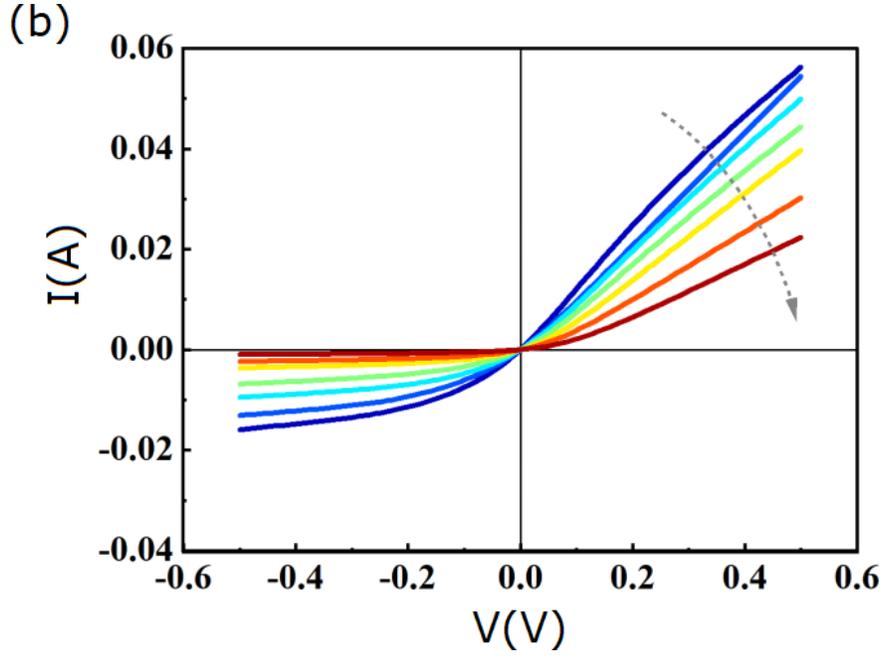
Figure 3 (a) Schematic diagram of the device for contact resistance measurement. (b) IV curves corresponding to c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag stacks with different electrode diameters. The arrow direction represents the electrode diameter decreasing.

Total resistance in ECSM can be expressed as:

$R_T = R_s + R_c + R_0$ (1)

where R_T is the total series resistance, R_s the extended resistance, R_c the contact resistance, and R_0 the residual resistance. R_T can be obtained by fitting the experimental I - V curve according to equation (2), where V is the applied voltage, I the current, n the ideal factor, q the electron charge, k the Boltzmann constant, and T the absolute temperature. R_s can be calculated from equation (3), where ρ and t are the resistivity and thickness of the Si substrate, respectively, d is the diameter of the circular electrode. ρ_s is the specific contact resistivity and can be obtained according to equation (4)[33].

(2)

(3)

(4)
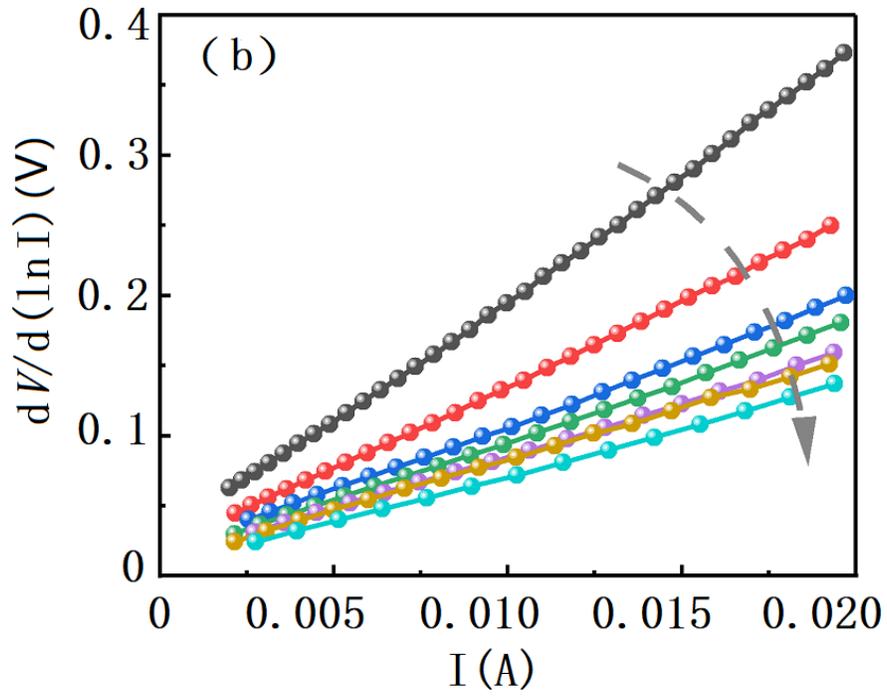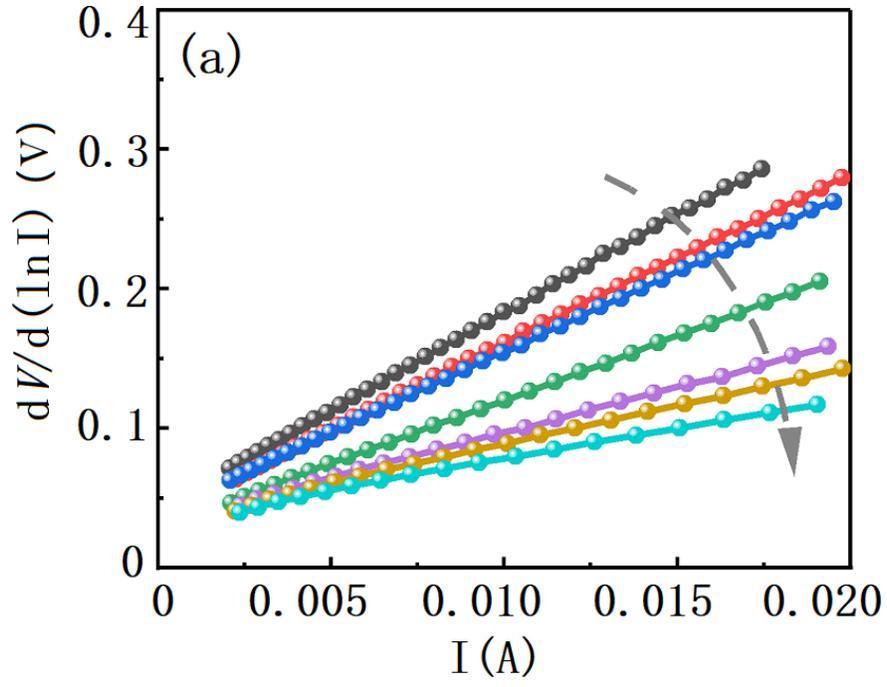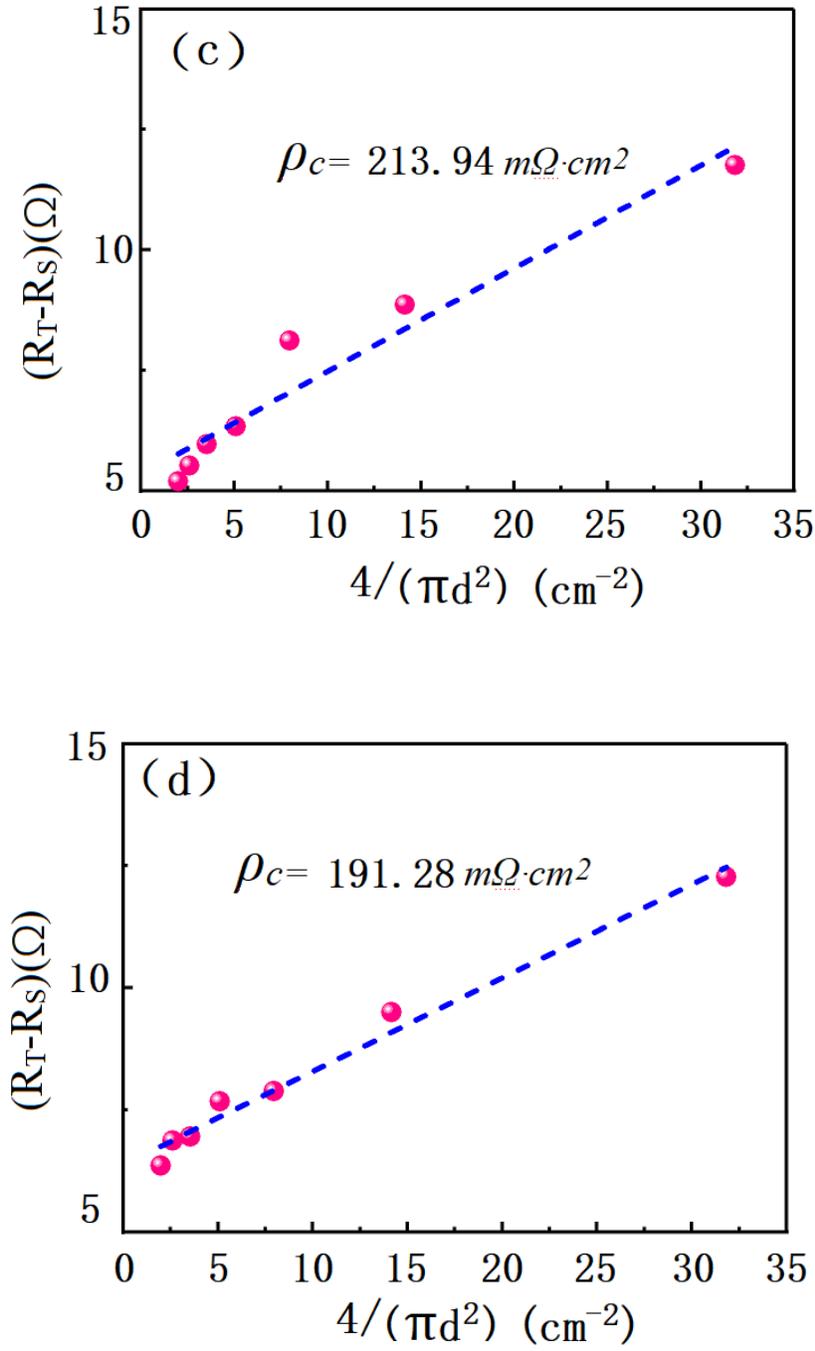
Figure 4 (a), (b) dV/d(lnI) versus I for a-Si:H(i)/MoO$_x$/Ag and a-Si:H(i)/MoO$_x$/ICO/Ag stacks with different electrode diameters. The arrow direction represents the electrode diameter decreasing. (c), (d) (R$_T$-R$_S$) versus $4/(\pi d^2)$ and the corresponding linear fitting curve.

Two stacks with the architectures of c-Si(p)/a-Si:H(i)/MoO$_x$/Ag and c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag were prepared for contact resistance measurement. The measurement and fitting results were depicted in Fig. 4.

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The calculated ρ_c of the c-Si(p)/a-Si:H(i)/MoO$_x$/Ag stack and the c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag stack is 213.94 mΩ·cm^2 and 191.28 mΩ·cm^2, respectively. It is worth noting that R_c contains not only the contact resistance between MoO$_x$ and ICO, but the one between MoO$_x$ and c-Si(p), and also the bulk resistances of each film layers. As far as the investigated two stacks, there architectures are the same except for the ICO layer. So the difference in ρ_c should come from the contact resistance of MoO$_x$/TCO and MoO$_x$/Ag. As a conclusion, in addition to improving long wavelength response as discussed previously, adding ICO between the MoO$_x$ and the Ag electrode can reduce the contact resistance as well.

3.3 Performance of large-area SCH solar cell

Using HWOSD to prepare MoO$_x$ HTL, the large-area (M6/166mm) MoO$_x$/c-Si(n) SCH solar cells with the front-contact back-junction structure were fabricated according to the optimal process flow as shown in Fig. 1. PV parameters of five SCH solar cells are shown in Table 1. The light J-V and EQE curves for the champion solar cell with V_{oc} of 709 mV, J_{sc} of 39.57 mA/cm^2, FF of 76.9 %, and PCE of 21.59 % are plotted in Fig. 5(a) and (b), respectively. As a reference, the light J-V and EQE of a SHJ solar cell with the same size as the SCH solar cells and with a PCE of above 25% are provided in Fig. 5. At present stage, all the PV parameters of the champion SCH solar cell are lower than those of the reference SHJ solar cell. The significantly lower FF could be partly attributed to the relatively high contact resistance between MoO$_x$ and ICO. The lower V_{oc} should be related to the screen printing and subsequent annealing process for preparing the Ag grids. This process is prior to the MoO$_x$ HTL deposition to avoid the deterioration of the MoO$_x$ layer caused by the 200°C annealing. Thereby, high-density defect states may appear at the a-Si:H(i)/MoO$_x$ interface due to the damage to the exposed a-Si:H(i) layer. The slightly lower I_{sc} is due to the slightly lower long wavelength EQE as can be seen in Fig. 5 (b). In order to improve the device performance, the development of new TCO films that are beneficial for low contact resistance, and a low-temperature grids process capable of avoiding MoO$_x$ deterioration are urgently needed. The potential V_{oc} of up to 752 mV under 1 sun illumination indicates the performance potential for further development of the SCH solar cells(Figure S1) .

Table 1 Performance parameters of large-area MoO$_x$/c-Si(n) SCH solar cells

Sample	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	PCE(%)
1	706	37.48	78.53	20.85
2 3 4 5	707 704 712 709	36.96 38.94 37.86 39.57	79.41 77.43 78.11 76.90	20.74 21.24 21.05 21.59
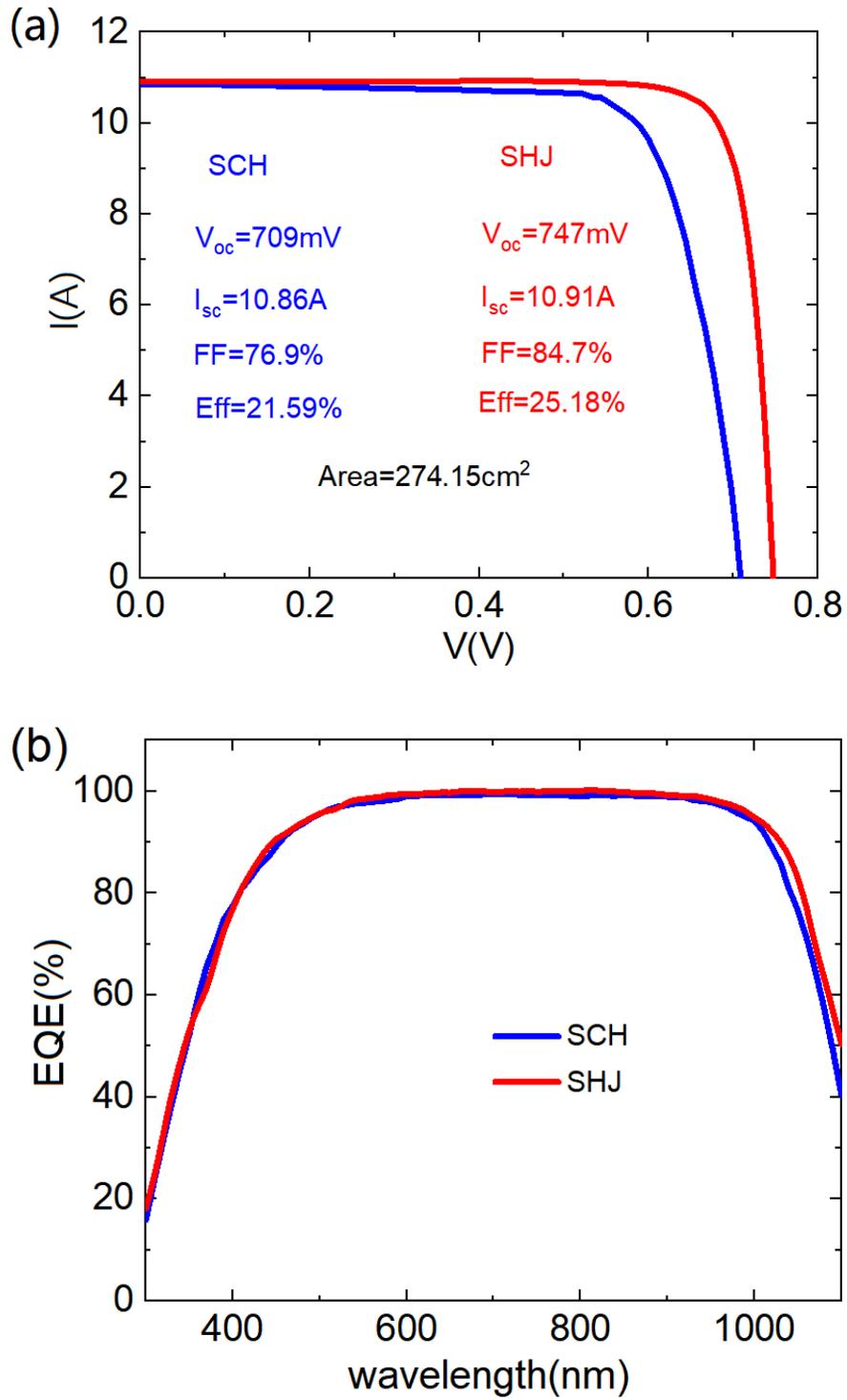
Figure 5 Light J-V (a) and EQE (b) curves of the champion MoO_x /c-Si(n) SCH solar cell and the reference SHJ solar cell with the same area of 274.15 cm^2.

Stability investigation

Stability tests were performed for the SCH solar cells with two kinds of rear architectures of c-Si(p)/a-Si:H(i)/MoO$_x$/ICO/Ag and c-Si(p)/a-Si:H(i)/MoO$_x$/Ag. Both solar cells are not encapsulated and stored in an air environment with a humidity of approximately 40% RH. The results are illustrated in Fig. 6. The thin MoO$_x$ film layer (~10 nm) is very sensitive to environment such as temperature and atmosphere[34,35]. Thereby, efficiency of the SCH solar cell with the rear structure of c-Si(p)/a-Si:H(i)/MoO$_x$/Ag rapidly decays from above 20.12% to 16.89% in 20 days (decays 16%). However, by inserting an ICO layer between MoO$_x$ and Ag, the ICO layer helps to protect the MoO$_x$ film and then the device stability improves significantly (decays 1.8%).
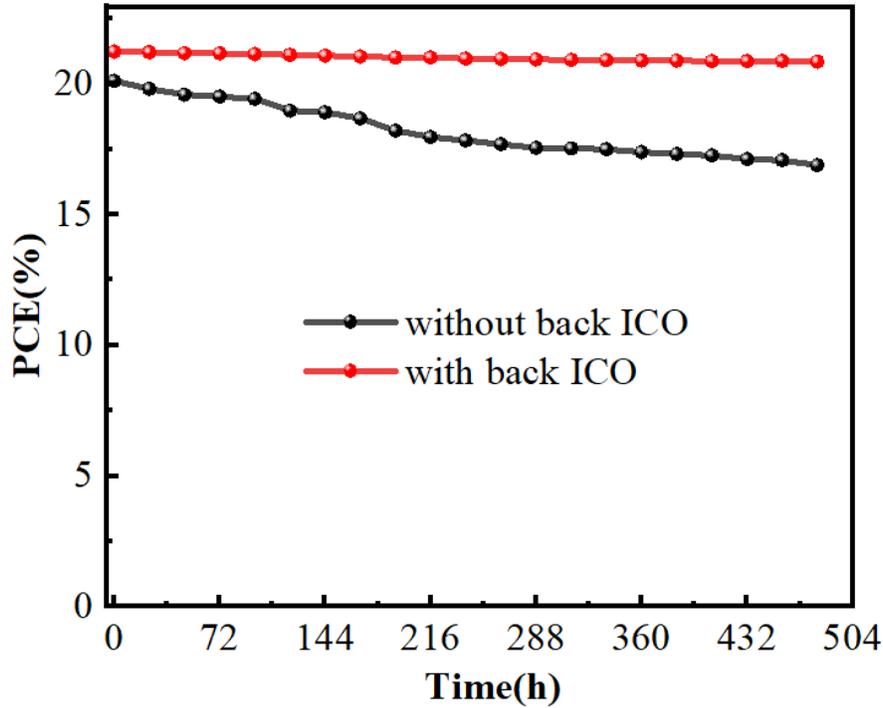
Figure 6 Efficiency stability measurement of SCH solar cell with and without back ICO layer

Depositing Ag back electrode directly on the MoO$_x$ film makes the fabrication process simple for the MoO$_x$/c-Si(n) SCH solar cell with a front-contact back-junction structure. However, adding a TCO layer between them is helpful and imperative for improving J$_{sc}$, reducing contact resistance, and improving device stability.

4 Conclusions

Large-area MoO$_x$/c-Si(n) SCH solar cells (M6 wafer) with a front-contact back-junction structure and with a ICO/Ag stack as the back reflector were fabricated according to the optimized fabrication process. Inserting ICO with a suitable thickness of 110 nm between MoO$_x$ and Ag effectively improves EQE in the long-wavelength, reduces the contact resistance, and improves the stability of the SCH solar cells. A power conversion efficiency of 21.59% is achieved on the champion SCH solar cell with the device area of 274.15 cm^2.

It was found that, although screen printing the metal grids before depositing MoO$_x$ layer is beneficial to prevent the deterioration of MoO$_x$ due to high temperatures, the fabrication process is not conducive to reducing the interface defects. Developing low-temperature metal grids technique is essential for improving the performance of large-area SCH solar cells.

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