Optimized recess etching criteria for T-gate fabrication achieving f_t= 290 GHz at L_g= 124 nm in metamorphic HEMT with $In_{0.7}Ga_{0.3}As$ channel

Jong Yul Park[1], Byoung-Gue Min[1], Jong-Min Lee[1], Woojin Chang[1], Dong Min Kang[1], E-San Jang[1], Junhyung Kim[1], and Jeonggil Kim[1]

[1]Electronics and Telecommunications Research Institute

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Abstract

We propose criteria for recess etching to fabricate T-gate used in InGaAs HEMTs. By patterning additional rectangular pads on the source and drain metals in the e-beam lithography step, it is possible to measure the drain-to-source resistance (R_{ds}) and current (I_{ds}). the ratio (Γ) of before and after etching for each R_{ds} and I_{ds} can be used as criteria to determine the point in time to stop etching. By performing recess etching with Γ= 1.97 for R_{ds} and Γ= 0.38 for I_{ds} on an epiwafer having cap doping concentration of 2= 10^{19} cm^{-3} and channel indium content of 0.7, we have fabricated InGaAs mHEMT device showing $g_{m,max}$= 1603 mS/mm and f_t= 290 GHz at L_g= 124 nm. The criteria presented can be applied to InGaAs HEMTs with various epitaxial structures.

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[1]Terrestrial and Non-Terrestrial Integrated Telecommunications Research Laboratory/Electronics and Telecommunications Research Institute, Yuseong-gu, Daejeon 34129, Republic of Korea

Email: jongyulpark@etri.re.kr.

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Introduction: Metamorphic high electron mobility transistor (mHEMT) with InGaAs channel material based on GaAs substrate can be applied to monolithic microwave integrated circuit (MMIC) with high frequency [1,2]. Compared to the competing InP-based InGaAs HEMT [3,4], the mHEMT exhibits relatively lower performance but is more cost-effective due to cheaper substrate price, the ability to fabricate on larger wafers, and ease of handling [5]. Both InP-based HEMT and GaAs-based mHEMT can have various epitaxial structures, mainly differentiated by the presence or absence of an InP layer between the cap and barrier

layers. Here the InP layer acts as an etch stop layer during recess etching process. After finishing recess etching, gate metal stacks of Pt/Ti/Pt/Au are usually deposited on InP layer [6] or InAlAs barrier [7]. In this case, however, it is essential to optimize parameters such as the thickness of the bottom Pt layer and Pt sinking temperature [8]. On the other hand, not using an InP etch stop layer can avoid such issues, but there is a risk of etching into the channel during recess etching process. To solve this problem, it is necessary to measure the drain-to-source resistance (R_{ds}) and current (I_{ds}) before and after etching to find proper time to stop etching process. It can be done by developing additional recess pads on source and drain metals, which are coated by e-beam resists. In our previous works, we dealt with the uneven recess etch rate between fingers in multi-finger mHEMT [9] and the etching depth variation according to the foot width of the T-gate [10].

In this paper, we present criteria of performing citric acid-based electrochemical recess etching before T-gate metal evaporation to fabricate high-performance InGaAs HEMTs. We describe the fabrication process from mesa isolation to e-beam lithography for T-gate pattern formation, followed by the recess etching process. Based on the measurement results of transconductance (g_m) and cut-off frequency (f_t), we emphasize the importance of the ratios (Γ) of before and after etching forR_{ds} and I_{ds} , which are criteria for optimization of recess etching. These criteria can be applied to InGaAs HEMTs with various epitaxial structures.

Fabrication process before recess etching: To fabricate InGaAs HEMT device, we used 4-inch GaAs substrate and molecular beam epitaxy (MBE) to grow epitaxial structures as shown in Table 1. First, metamorphic buffer layer, which was used to offset the lattice mismatch between GaAs and $In_{0.52}Al_{0.48}As$ buffer layer, was grown on semi-insulating GaAs substrate by changing its In content (x) from $x = 0$ to 0.52. Then, $In_{0.7}Ga_{0.3}As$ of 10 nm was formed to be used as a channel on $In_{0.52}Al_{0.48}As$ buffer layer of 300 nm. The carrier density and channel mobility ($\mu_{S\eta}$) were $2.9\times10^{12}cm^2$ and 10710 cm^2/V[?]s, respectively. Next, Si δ-doping of 6×10^{12} cm^{-2} was applied to supply electrons to the channel upon $In_{0.52}Al_{0.48}As$ spacer of 3 nm. Another Si δ-doping of 5.5×10^{12} cm^{-2} was applied in $In_{0.52}Al_{0.48}As$ barrier to enhance conductivity. Finally, $In_{0.53}Ga_{0.47}As$ cap layer of 20 nm doped with Si of $2x10^{19}$ cm^{-3} was formed on $In_{0.52}Al_{0.48}As$ barrier to fabricate Ohmic contacts of source and drain electrodes. The epitaxial structure designed by our research group was produced by IntelliEPI Inc. and its sheet resistance was 77.8 Ω/sq. By using this 4-inch epiwafer, mesa isolation was firstly conducted. Each HEMT device were separated by mesa having thickness of 200 nm, which were etched by solution of H_3PO_4:H_2O_2:H_2O= 1:1:40. As a result of transmission line measurement (TLM) with a gap of 5 μm between 100×100 μm mesa pads, 61 GΩ was measured, and 65 pA was flowed at 2 V, which confirms that mesa-to-mesa isolation was properly achieved.

Table 1: Epitaxial structure of InGaAs HEMT.

Layer	*Material*	*THK*	*Level*	*Type*
cap	$In_{0.53}Ga_{0.47}As$	20 nm	$2.0\times10^{19}/cm^3$	N+
barrier	$In_{0.52}Al_{0.48}As$	2 nm	-	i
1st δ-doping	Si	-	$5.5\times10^{12}/cm^2$	N
barrier	$In_{0.52}Al_{0.48}As$	6 nm	-	i
2nd δ-doping	Si	-	$6.0\times10^{12}/cm^2$	N
spacer	$In_{0.52}Al_{0.48}As$	3 nm	-	i
channel	$In_{0.7}Ga_{0.3}As$	10 nm	-	i
buffer	$In_{0.52}Al_{0.48}As$	300 nm	-	i
m-buffer	GaAs -$In_{0.52}Al_{0.48}As$	300 nm	-	i

To fabricate Ohmic contact serving as a source and drain, Mo/Ti/Pt/Au, each with thickness of 10/30/30/280 nm, was deposited by using e-beam evaporator. The source-to-drain distance of the device was designed to be 2 μm. Also, the device was designed as a two-finger T-gate with a total gate width of 100 μm. To measure the resistance of Ohmic contact, patterns with interval of 5/10/20/40/80 μm were made. As a result of TLM measurement, a contact resistance (R_c) of 0.078 Ω[?]mm was measured.

After coating PMMA-based tri-layer to make T-gate patterns, e-beam lithography using Raith EBPG 5000 was performed with 100 nm target for foot and 600 nm target for head, respectively. In addition, "anchor" and "gate pad" were added to the end of each T-gate pattern to ensure structural stability, as shown in Fig. 1a. After finishing to develop patterns, descum process was performed to remove residues so that the final foot width became about 120 nm.

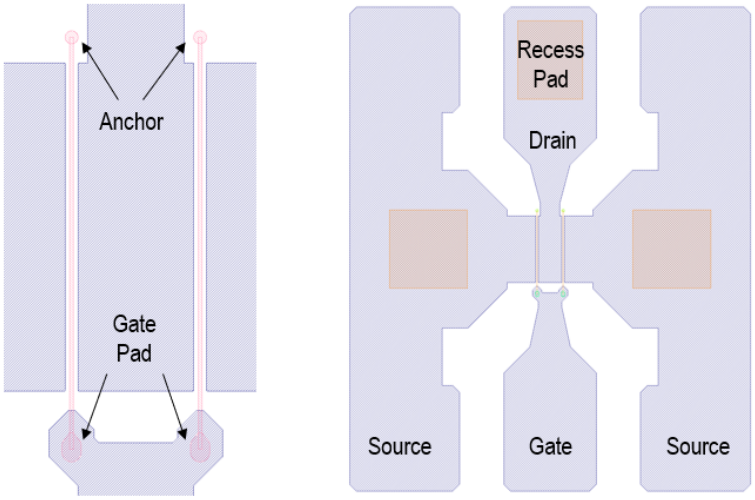

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Fig. 1 *Top views of design for HEMT device.*

a Anchor and gate pad added to the end of two-finger T-gate.

b Recess pads for monitoring R_{ds} andI_{ds} during recess etch process.

Gate recess etching: Before evaporating T-gate metal stacks, recess etching for InGaAs and InAlAs makes it possible to improve gate controllability so that higher g_m is secured. As shown in Fig. 1b, rectangular pads were additionally exposed on the source and drain metals in the e-beam lithography step [9,10]. These "recess pads" should have a size enough to contact probe tips. By using developed recess pads, it is possible to monitorR_{ds} and I_{ds} for biased drain voltage (V_D). Accordingly, it is feasible to find optimal point in time to stop etch and keep from etching of 2nd Si δ-doping layer on the $In_{0.52}Al_{0.48}As$ spacer. Also, by using citric acid-based etchant, InGaAs/InAlAs layers can be electrochemically etched because potential difference occurs between InGaAs/InAlAs layer opened by foot pattern and Ohmic metal opened by recess pad. In the same way as our previous paper [10], an etchant comprising citric acid (10 g), hydrogen peroxide (1 ml), and water (430 ml) was used and maintained its temperature at 32 C°.

To find an appropriate point in time to stop etching, we compared the experimental results for two different epitaxial structures, which have the same thickness of $In_{0.53}Ga_{0.47}As$ cap and $In_{0.52}Al_{0.48}As$ barrier/spacer, but differ in cap doping concentration (N_{cap}), the number of Si δ-doping layers, and In content of channel. Figure 2 shows the R_{ds} at $V_d = 0$ V and theI_{ds} at $V_d = 1$ V for these two epitaxial structures. Comparing R_{ds} andI_{ds} before etching for$N_{cap} = 1\times10^{19}$cm^{-3} (dash-dotted line, [10]) and$N_{cap} = 2\text{x}10^{19}$cm^{-3} (solid line, this work), highN_{cap} reduces R_{ds} and increases I_{ds} . The R_{ds}gradually increases as the thickness of the cap layer decreases by recess etching. Even if the cap layer is completely etched and InAlAs barrier is revealed, R_{ds} does not change abruptly and keep gradually increasing because Si δ-doping layers supply electrons to form current path.

In the previous work, we stopped to etch when$R_{ds} = 18.7\ \Omega$ and $I_{ds} = 31.3$ mA were measured, and the resultant device showed good performance [10]. Here the ratios (Γ) of before and after etching for eachR_{ds}

and I_{ds} can be defined in equations as follows:

, , (1)

where i = 0,1,2…,n is integer and n means the number of times etching has been performed. In the case of previous work, Γ_R = 1.82 and Γ_I = 0.39. Referring to these ratios, in this work, etching was stopped whenR_{ds} = 13 Ω and I_{ds} = 34.7 mA so that Γ_R = 1.97 and Γ_I = 0.38. Here, the Γ_R was adjusted slightly higher and the Γ_I was adjusted slightly lower, taking into consideration the additional 1st Si δ-doping layer and 0.7 of channel In content. Additionally, for another wafer with the same epitaxial structure as this work, more etching was carried out, resulting in a rapid change of R_{ds} = 21.1 Ω and I_{ds} =24.3 mA (dotted line) so that Γ_R = 3.34 and Γ_I = 0.26, which can be assumed to indicate etching down to the 2nd Si δ-doping layer. This led to a poor device operation of I_{on} ~ 10mA at V_d =0.8 V and g_m ~ 200 mS/mm.

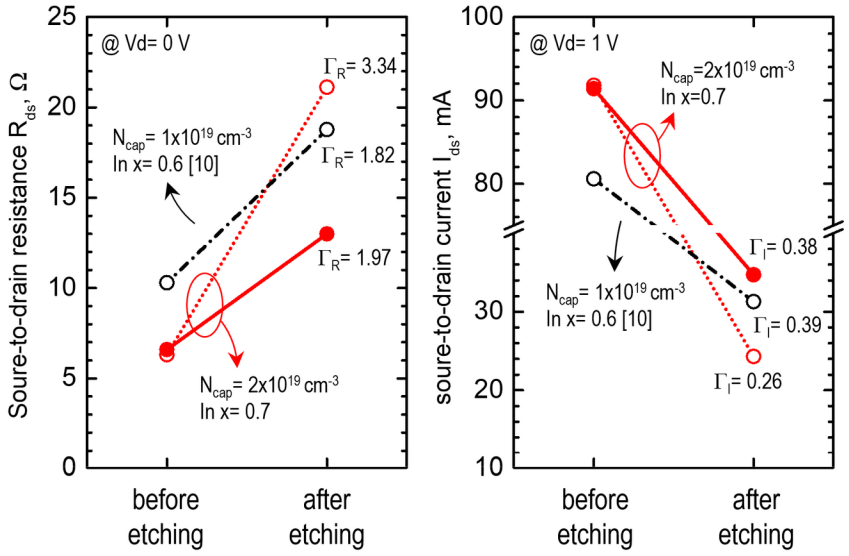

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Fig. 2 *Measurement results of R_{ds} and I_{ds} for mHEMTs having cap layer of N_{cap}= 1×10^{19} cm^{-3} and N_{cap}= 2x10^{19} cm^{-3}before and after recess etching process.*

a R_{ds} when biasing V_d = 0 V.

b I_{ds} when biasing V_d = 1 V.

Following the etching process, the gate stack of Ti/Au= 40/400 nm were evaporated. After finishing lift-off process, SiN of 50 nm was deposited by PECVD for passivation. Figure 3 shows the results of transmission electron microscopy (TEM) using Tecnai F30 S-Twin after completing T-gate fabrication. The final gate length (i.e., gate foot width) is evaluated as about 124 nm (see Fig. 3a), which is similar to the length examined by CDSEM after descum. By magnifying TEM to make the epitaxial structures more visible, it can be observed that $In_{0.7}Ga_{0.3}As$ channel on $In_{0.52}Al_{0.48}As$ buffer has thickness of 10 nm, as designed (see Fig. 3b). Above the channel, it is noticeable that the thickness of $In_{0.52}Al_{0.48}As$ remaining after recess etching is about 7.7 nm. This means that the T-gate was deposited on 4.7 nm from the 2nd Si δ-doping layer, so it can be evaluated that the recess etching was properly performed to suppress the occurrence of gate leakage current.

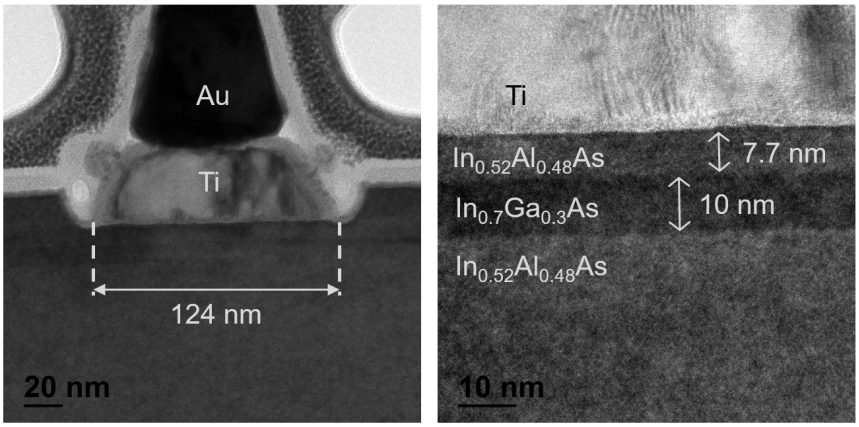

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Fig. 3

Cross-sectional TEM images.

a T-gate foot deposited on recessed $In_{0.52}Al_{0.48}As$ layer.

b Magnified TEM image showing epitaxial structures below T-gate foot.

Electrical characteristics: Figure 4 illustrates the device performances by measuring with Keysight HP4142 and Cascade on-wafer probe station. During the measurement, the biased drain voltage (V_d) was fixed at 0.8 V. As shown in Fig. 4a, when gate voltage (V_g) was biased at -1 V, drain current (I_d) was measured at 1.6 μA/mm. When biasing $V_g = 0.2$ V, the $I_d$was measured at 664.7 mA/mm. From the measurement results, the threshold voltage (V_{th}) and maximum transconductance ($g_{m,max}$) of -0.47 V and 1603 mS/mm were extracted, respectively. Subsequently, the S-parameter for the frequency range of 0.5-50 GHz was measured using a Keysight N5245A microwave network analyzer while $V_g = 0$ V and $V_d = 0.8$ V were applied to the same device. The result of calculating the current gain of h_{21} was shown in Fig. 4b. By extrapolating with a line of -20 dB/decade, 290 GHz of f_t was extracted.

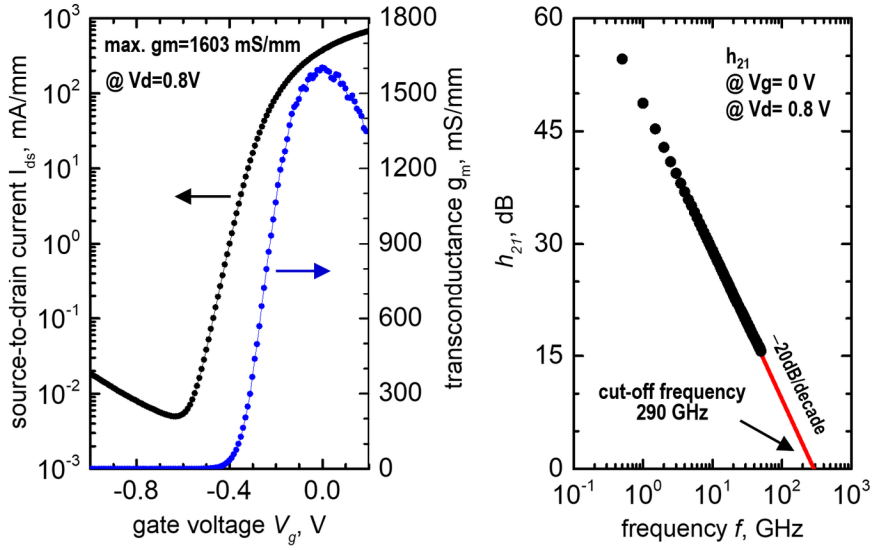

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Fig. 4 *Electrical characteristics of mHEMT.*

a Measured V_g-I_{ds} plot and extracted g_m curve at $V_d = 0.8$ V.

b Calculated h_{21} and extrapolated line to find f_t.

Figure 5 describes comparison between these results (f_t and $g_{m,\ max}$) and the other values reported by various research groups. All references dealt with mHEMTs for channel In x range from 0.6 to 0.8. Firstly, we obtained higher cut-off frequency of 290 GHz at longer gate length of 124 nm compared to the results of our previous work (f_t = 210 GHz at L_g = 100 nm, [2]). Considering that recess etching was carried out properly for both devices, the one of the main reasons for the difference in performance is epitaxial structure changed its channel In content from 0.6 to 0.7 and N_{cap} from$N_{cap} = 1\times10^{19}$cm^{-3} to $N_{cap} = 2\text{x}10^{19}$ cm^{-3}.

Next, in comparison with the results from other research groups, thef_t = 290 GHz obtained in this paper is higher than that of devices with L_g = 100 nm [11] andL_g = 80 nm [7], which havef_t values of 220 GHz and 246 GHz, respectively. Also, the f_t performance in this paper is comparable to the device reporting f_t = 293 GHz atL_g = 70 nm [12]. To analyse the reasons, it is necessary to perform a detailed analysis for each case because different epitaxial structures or device designs were used by each research group. However, a simple overview of all cases reveals that, as shown in Fig. 5b, our result shows relatively high $g_{m,max}$ = 1603 mS/mm, which leads to the high f_t value according to the equation of $f_t = g_m /2\pi(C_{gs} + C_{gd})$. Hence, it can be evaluated that the optimal recess etching performed in this study led to a sufficient g_m potentially achievable by the device design and epitaxial structure.

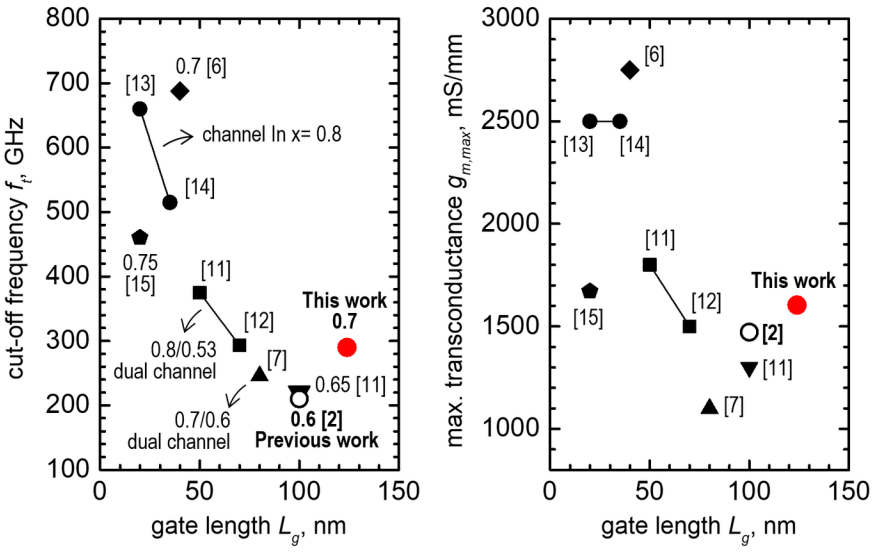

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Fig. 5 *Comparison our results in this paper with other reported values for mHEMTs with In x range of 0.6-0.8.*

a L_g-f_t plot for results comparison.

b L_g-$g_{m,max}$ plot for results comparison.

Conclusion: We have demonstrated the recess etching technique for T-gate fabrication in InGaAs mHEMTs. By opening additional recess pads on the source and drain metals, it is possible to find the optimal point in time to stop etching by measuring R_{ds} andI_{ds} . Specifically, by referring the criteria of Γ_R = 1.82 and Γ_I

= 0.39 for epiwafer having N_{cap} = 1×10^{19}cm^{-3} and channel In x = 0.6, we have adjusted the criteria and performed recess etching to be Γ_R = 1.97 and Γ_I = 0.38 for epiwafer having N_{cap} = 2×10^{19}cm^{-3} and channel In x = 0.7. As a result, we have fabricated mHEMT device showing $g_{m,max}$ = 1603 mS/mm and f_t = 290 GHz atL_g = 124 nm. Even with different epitaxial structures, referring to the criteria of Γ_R and Γ_I ratios presented in this paper would be helpful to find the appropriate timing to stop recess etching for successful fabrication of InGaAs HEMTs.

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