A 0.9 V Wideband SPLL With an Adaptive Fast-Locking Circuit Achieving 24.68 μs Settling Time Reduction

Binghui Wang[1], Shu Zhou[2], and Hai-Gang Yang[3]

[1]Chinese Academy of Sciences Aerospace Information Research Institute
[2]Nanyang Technological University School of Electrical and Electronic Engineering
[3]University of the Chinese Academy of Sciences

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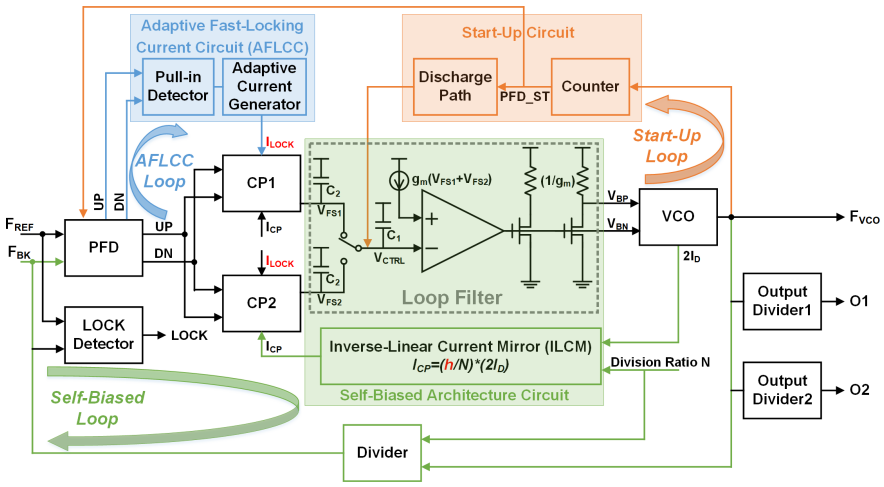
Abstract

A low-power wideband self-biased phase-locked loop (SPLL) is proposed for multi-protocol SerDes applications in this letter. With the proposed adaptive fast-locking current circuit (AFLCC), the settling time is reduced significantly, and no extra power and jitter contribution. In addition, a start-up module is adopted to reset the system to an optimal initial operating frequency quickly. The proposed 1-3-GHz SPLL, fabricated in TSMC 28-nm CMOS process and occupies a compact 0.028mm2 area. It achieves a roughly constant settling time of 5 μs over all frequencies and division ratios range. Only 0.96 mW is consumed from a 0.9 V supply at 1 GHz frequency.



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Binghui Wang [1,2], Zhou Shu [3], and Haigang Yang [4]

[1] *Aerospace Information Research Institute, Chinese Academy of Sciences, Beijing 100190, China*

[2] *School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100094, China*

[3] *School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore*

[4] *School of Microelectronics, University of Chinese Academy of Sciences, Beijing 100049, China*

Email: wangbinghui18@mails.ucas.ac.cn

A low-power wideband self-biased phase-locked loop (SPLL) is proposed for multi-protocol SerDes applications in this letter. With the proposed adaptive fast-locking current circuit (AFLCC), the settling time is reduced significantly, and no extra power and jitter contribution. In addition, a start-up module is adopted to reset the system to an optimal initial operating frequency quickly. The proposed 1-3-GHz SPLL, fabricated in TSMC 28-nm CMOS process and occupies a compact 0.028mm^2 area. It achieves a roughly constant settling time of 5 μs over all frequencies and division ratios range. Only 0.96 mW is consumed from a 0.9 V supply at 1 GHz frequency.

Introduction: P hase-locked loops (PLLs) are essential blocks in serialize/deserialize interfaces (SerDes). As the development of SerDes, PLLs should be designed with lower jitter, faster locking, and wider bandwidth to facilitate agile operation. Furthermore, communication standards like SATA 2 and USB 3.0 require the use of spread spectrum clocking, which can cause significant frequency variations. As a result, PLLs must meet more stringent lock and jitter requirements over process, voltage, and temperature (PVT) variations.

Among analog PLLs, SPLLs have been widely investigated for their constant damping factor and adaptive bandwidth, which are independent of PVT. To reduce power consumption and phase noise, low-power source-degeneration voltage-to-current converters are adopted in [1]. However, the lock time is not improved because its loop bandwidth cannot scale with the input frequency. Adaptive bandwidth control techniques are attractive for facilitating the locking process and have been used in ring-oscillator-based self-biased PLLs [2-3], but the locking latency caused by the large division ratio effect still exists. Although, [4] provides an initialization circuit to speed up the VCO oscillation, reducing power-up latency is challenging, particularly when the target frequency is low.

This letter proposes an AFLCC to accelerate the loop settling over all tuning frequencies and all division ratios. To enhance the robustness and acceleration, a start-up circuit is adopted to guarantee the initial frequency is located at the middle of the tuning range. As a result, settling time is significantly improved with little power and area penalty.

Self-biased loop description: The block diagram of the proposed SPLL is shown in Fig. 1, which consists of three loops: the self-biased loop, AFLCC loop, and start-up loop. The SPLL supports a multiplexer of 5-511 and employs an output divider (2-30) to provide a multi-phase clock that is compliant with various wireline standards. The SPLL can be treated as a second-order system, where the bandwidth ω_N and damping factor ζ are the key parameters.

Compared with the typical analog PLLs, the resistor in the loop filter is replaced by a $\frac{1}{g_m}$ resistance, a sampled filter circuit is adopted, and the charge pump current I_{CP} is set to the multiplied $\frac{(1}{N)}$ of the VCO buffer tail current $2I_D$ by an inverse-linear current mirror circuit (ILCM). These ways make damping factor ζ and$\frac{\omega_N}{\omega_{\mathrm{ref}}}$ constant and given by (1), (2)

$$I_{\mathrm{CP}} = \frac{1}{N}\left(2I_D\right) \tag{1}$$

$$\frac{\omega_N}{\omega_{\mathrm{ref}}} = \frac{1}{2\pi}\sqrt{\frac{C_B}{C_1+C_2}}\ ,\ \zeta = \frac{1}{4}\frac{\sqrt{C_B(C_1+C_2)}}{C_2} \tag{2}$$

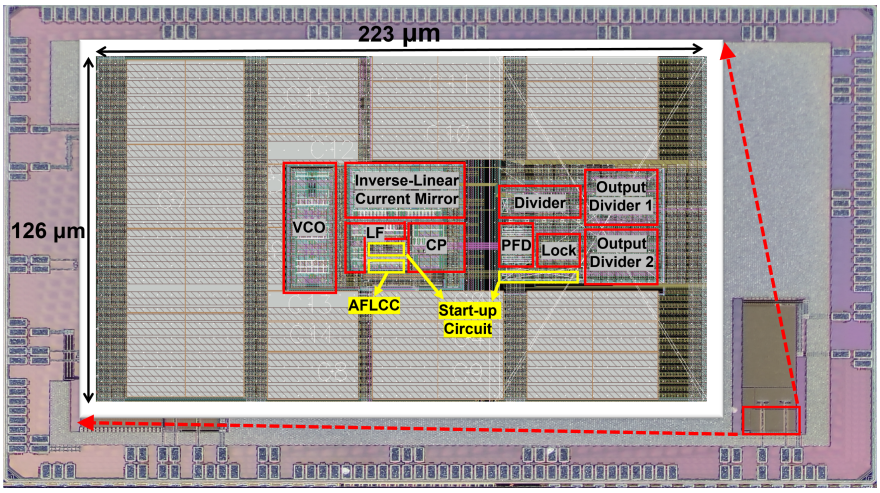
where C_B is the equivalent capacitance of the VCO, C_1andC_2 are capacitors in the sampled filter circuit. Therefore,$\frac{\omega_N}{\omega_{\mathrm{ref}}}$ and ζ hold independent of division ratios N, VCO frequency and PVT.

Proposed AFLCC loop and circuit : In typical SPLLs, the pull-in process becomes slower as the N increases.

This is problematic for wideband communication applications, where the value of N can vary greatly. To reduce the locking time over large N, the AFLCC based on bandwidth tracking and adaptive current injection is proposed. During the settling process, this AFLCC injects an extra currentI_{LOCK} into the CP to widen the bandwidth.I_{CP}, I_{LOCK} are adaptive and can be determined using Equation (3). For more flexibility in circuit optimization, the coefficient $(\frac{1}{N})$ is updated to (h/N).

$$I_{\mathrm{LOCK}} = k_1 (2I_D) = \frac{k_1 N}{h} I_{\mathrm{CP}} \ , \ I_{\mathrm{CP}} = \frac{h}{N} (2I_D) \quad (3)$$

$$\frac{\omega_N}{\omega_{\mathrm{ref}}} = \sqrt{h + k_1 N} \left(\frac{\omega_N}{\omega_{\mathrm{ref}}} \right)_0 , \quad \zeta = \sqrt{h + k_1 N} \zeta_0 \quad (4)$$



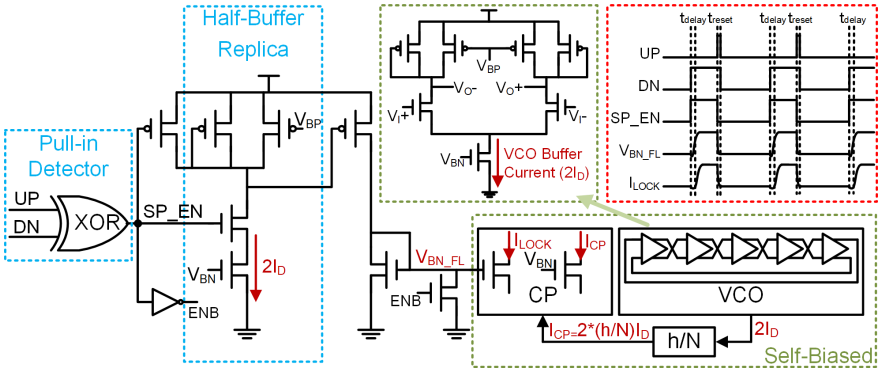
Assuming the original steady-state parameters to be ζ_0 and$(\omega_N/\omega_{\mathrm{ref}})_0$, both parameters in the pull-in process will be enlarged by $\sqrt{h + k_1 N}$ (4), furthering to widen the bandwidth and accelerate the acquisition. When in the locked state, I_{LOCK} is cut off, so the CP current is recovered to an optimized value for the optimal bandwidth. Therefore, the AFLCC has no implication whatsoever on the steady behavior of the loop.

Fig. 2 shows the structure and working principle of the AFLCC. The half-buffer replica can precisely track I_D to keepI_{lock} up to date. The pull-in detector generates a variable-width pulse (SP_EN) according to the outputs of the PFD. As a result, the I_{LOCK} is adaptive on the 'width' in effect. Additionally, due to non-ideal switch behavior, there is a tiny delayt_{delay} in the output. Intuitively, the AFLCC takes time to charge V_{LCPNBS} away from 0, so do I_{lock}. So, if the phase error gets smaller than a certain level, the AFLCC will not be activated at all. The intrinsic delay makes the AFLCC turn off a little earlier than the locked point is reached. This characteristic benefits the settling behavior especially for the cases of high reference frequency or of the loop getting close to the locked state. Fig. 3 displays the whole pull-in sequence, where the loop acquisition is accelerated remarkably due to the AFLCC.

Start-up loop and circuit: The fast start-up stage in Fig.3 is contributed by the start-up circuit and holds a short duration. When the SPLL is reset,V_{CTRL} start dropping from the supply voltage through the discharging path in the start-up circuit. Until V_{CTRL}falls to the start voltage of the oscillator, the counter is activated and serves to decide if the VCO has reached a continuous oscillation. When satisfied, the counter asserts the flag signal PFD_ST, the start-up circuit is disabled, and the PFD is activated. These push the system into the loop acquisition stage.

For this ring oscillator, its start voltage keeps fixed (˜0.6 V), as shown in Fig.3, which is located on the left side of the linear region of the K_V curve with a lowerK_V value, so do the loop gain and bandwidth. As a rule of thumb, it is wise to situate the loop start point in the middle of the linear region. Therefore, the

counter is utilized to extend the discharging time and push the loop start point to the left until it is shifted near the middle of the linear region, as shown in Fig.3. The larger loop gain and bandwidth on the loop start point help to accelerate the settling process but also guarantee the robustness of the system.



The different periods (N_C) of the counter are the key factor and decide the distance between the VCO start and loop start point, which leads to varied locking times. Its optimal value is given by (6), whereτ is the time constant of discharging, f_0 andf_{op} are the initial and middle frequency of VCO respectively, t_0 and t_{op} are the corresponding value to f_0 and f_{op} on the voltage-time discharging curve of V_{CTRL}. The Nc is set to 64 cycles here.

$$N_C = \frac{f_0+f_{\text{op}}}{2} * \text{VDD} * \left(e^{-\frac{t_0}{\tau}} - e^{-\frac{t_{\text{op}}}{\tau}}\right) \quad (6)$$

*Experimental Results:*The proposed SPLL was fabricated in TSMC 28-nm CMOS. Fig. 4 displays the die photo and the active area of the proposed SPLL is 0.028 mm^2. The total area of the AFLCC and start-up circuit is 260 μm^2, only 0.93% of the core area. Fig. 5 shows the transient waveforms of the typical SPLL and proposed SPLL withF_{VCO} at 2 GHz and N at 500. Their settling times are 28.96 µs and 4.28 µs, respectively, and their start-up stages hold a similar duration of about 700 ns, and the loop acquisition is accelerated by 85% remarkably.

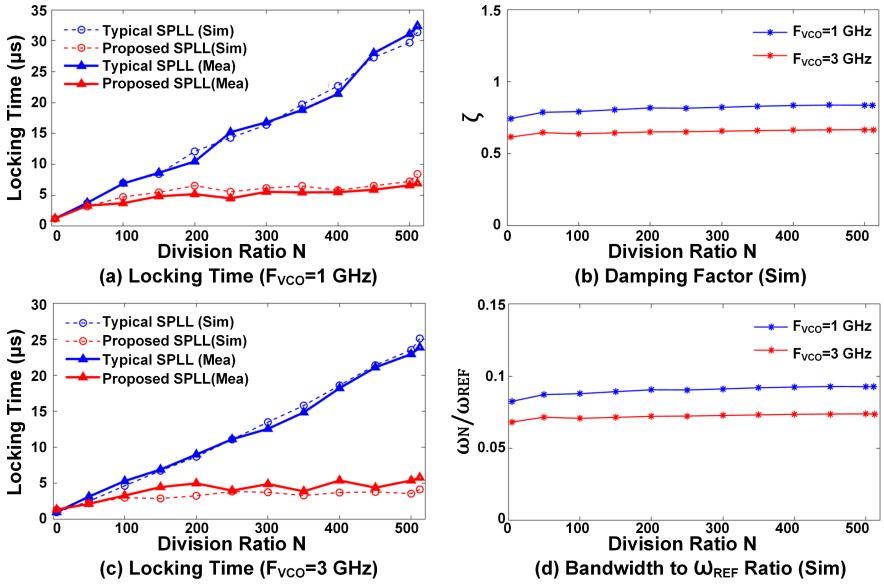
To further verify the overall fast-locking performance, the simulated and measured settling times are shown in Fig. 6(a) and (c), which show good consistency. It's noted that the loop acquisition exhibits non-linear behavior, so all measured data presented here is an average value under the same conditions. The results indicate that the locking time of the typical SPLL increases with the larger value of N, while the proposed SPLL significantly reduces the locking time and pushes it to a similar value (˜5 µs). Two dynamics parameters,ζ and $\omega_N/\omega_{\text{ref}}$, were simulated and shown in Fig 6(b) and (d), which remain roughly constant at about 0.7 and 0.08, respectively. The tiny deviations at the same N are induced by the inaccuracies of the ILCM.

The measurements show that the power consumption difference between the typical SPLL and the proposed SPLL is less than 9µW, which reveals the tiny power dissipation overhead of AFLCC. The power consumption increases from 0.96mW to 5.46mW as the operating frequency ranges from 1 to 3 GHz. The dissipation includes the test modules, such as differential signaling input buffers, isolators, etc. Fig. 7 shows the phase noise and jitter of the typical and proposed SPLL at 2 GHz VCO frequency with N equal to 125. The phase noises at 1 MHz offset were about –93.89 dBc/Hz and –94.82 dBc/Hz, respectively. And the time-domain measurements of clock jitters were 2.29 ps and 2.33 ps, respectively. It indicates that the AFLCC did not significantly deteriorate the phase noise and jitter performance.

Table I compares the proposed SPLL with the state-of-the-art PLLs [5-9]. The proposed SPLL improves the

settling time at expenses of small area overhead. The tuning range and division ratio range are relatively wider, and good power efficiency is achieved.

Conclusion: This letter demonstrates a 1-to-3 GHz fast-locking and low-power SPLL fabricated in 28 nm CMOS. The proposed adaptive fast-locking scheme maintains a reduced settling time with tiny power and area overhead. Moreover, a start-up module is adopted to further reduce loop latency and increase system robustness. The measured RMS jitter is 2.33 ps. Therefore, this proposed SPLL is an effective solution for various wireline standards. For example, in USB 3.0 (5Gbps) standard, total jitter budget of the transmitter is 75 ps.



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