Fully Passive Noise-Shaping SAR ADC Realizing 2X Passive Gain Without Capacitor Stacking

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Abstract

The fully passive noise shaping (NS) successive approximation register (SAR) analog-to-digital converters (ADCs) are simple, OTA-free and scaling friendly. Previous passive NS-SAR ADCs rely on the multi-path-input comparator or capacitors stacking to realize the passive gain for compensating the signal attenuation during passive integration. However, the former causes high comparator power consumption, and the latter suffers from additional signal attenuation due to the parasitics and is hard to extend to high-order systems. This work proposes a new fully passive NS-SAR technique, it can realize 2× gain with a simple structure, leading to the reduced comparator power and less parasitics. This technique is also easy to extend to high-order NS-SAR ADCs.

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The fully passive noise shaping (NS) successive approximation register (SAR) analog-to-digital converters (ADCs) are simple, OTA-free and scaling friendly. Previous passive NS-SAR ADCs rely on the multi-path-input comparator or capacitors stacking to realize the passive gain for compensating the signal attenuation during passive integration. However, the former causes high comparator power consumption, and the latter suffers from additional signal attenuation due to the parasitics and is hard to extend to high-order systems. This work proposes a new fully passive NS-SAR technique, it can realize 2× gain with a simple structure, leading to the reduced comparator power and less parasitics. This technique is also easy to extend to high-order NS-SAR ADCs.

Introduction: The NS-SAR ADC is an emerging ADC architecture that aims to combine the benefits of both SAR and $\Delta\Sigma$ ADCs while simultaneously obviating their drawbacks [1-6]. There are three types of NS-SAR ADCs in general. The first one is to use the closed-loop operational transconductance amplifiers (OTAs) to realize the active integrators, but OTAs consume high static power [1]. The second one uses the open-loop dynamic amplifier to reduce power consumption [2]. However, the gain of dynamic amplifier is sensitive to process, voltage, and temperature (PVT) variations. The last one is the passive NS-SAR ADCs which do not consume static power and are PVT robust. Nevertheless, the passive NS-SAR ADCs also have their own limitations.

Previous passive NS SAR: In [3], the second-order NS SAR ADC samples the residual voltage on the capacitive digital-to-analog converter (CDAC) through a small residual capacitor, and then uses the sampled residue voltage to complete the first- and second-order integrations in turn. However, the small residue

capacitor introduces a large kT/C noise. Besides, in order to compensate for the signal attenuations during residue sampling and passive integrations, the multi-path-input comparator needs to provide large path gains. To realize the NTF of $(1\text{-}0.75z^{-1})^2$, the comparator path gain ratio needs to be 1:4:16. For the same noise budget, the comparator power consumption is 441× larger than that of a single-path-input one. The work in [4] removes the residue sampling operation, greatly reducing the kT/C noise. It also reduces the comparator path gain ratio to be 1:3:12, leading to the reduced comparator power of 256× larger than that of a single-path-input one. However, the comparator power is still too large, which often dominates the total ADC power and restricts the NS-SAR to be extended to higher-order. In [5], the integration capacitor is split into 2 parts and stacked after the integration. In theory, it can realize 2× passive gain, and therefore the comparator path ratio can be reduced by nearly half. However, the capacitor stacking causes additional signal attenuation due to the parasitics from the capacitor plates, which can be a large portion of the effective capacitor. The work in [6] uses the capacitor stacking to realize 4× passive gain, and only requires a single-path-input comparator. Also, by the differential integration, it can reduce the integration capacitors by 4× than [4] and [5]. However, it also suffers from the signal attenuation caused by the capacitor stacking, and which can be more severe than [5] because its complex switch network. Besides, it is difficult to extend this technique to higher-order NS due to the severe parasitics.

Proposed passive NS SAR with 2× gain: Inspired by the above NS SAR techniques, this paper proposes an integration circuit to achieve 2× passive gain in a simple manner. As shown in Fig. 1, the integration capacitor is split into two parts. During the integration phase, the two parts are connected in parallel between the two CDACs for differential integration, the obtained integration voltage is denoted as V_{int}, as shown in Fig. 1a. After integration, the bottom plates of the two parts are grounded, and therefore, the differential voltage between their top plates is obtained as $2V_{int}$, as shown in Fig. 1b. In this way, the 2× passive gain is realized. It can be seen that the circuit is simple and does not need capacitor stacking.

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a

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b

Fig.1 *Proposed integration circuit*

a During integration

b After integration

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Fig.2 *Proposed NS SAR schematic and timing*

Based on the proposed technique, a second-order NS-SAR ADC is designed, as shown in Fig. 2. After the normal SAR conversion, the first- and second-order differential integrations take place in run. After each integration, the bottom plates of the integration capacitors are grounded to realize the 2× passive gain. The top-plates of the integration capacitors are connected to the comparator inputs. A 3-path-input comparator is used as the adder in the feedforwad path and also provides the required gains for the integration signals. As there is already 2× gain realized in the passive integrator, the required comparator gains for the integration

paths can be reduced by half. To realize the NTF of $(1\text{-}0.75z^{-1})^2$, the required path gain ratio is 1:1.5:6. For the same noise budget, the comparator power consumption is 72.25× of that of a single-path-input one.

Table 1 summarizes the capacitor size and comparator gain ratio of this work, and compares them with the prior work [3] and [4] for the same kT/C noise and comparator noise budget. Both of the three works realize the NTF of $(1\text{-}0.75z^{-1})^2$. The work [3] suffers from the significant residue sampling noise, resulting in the large CDAC size. The work [4] obviates the residue sampling noise, and therefore it can reduce the CDAC size by 5× and reduce the total capacitor size by 2.4×. Comparing to [4], this work reduces the integrator capacitor size by 4× by using the differential integrations, and reduces the total capacitor size by 2.8×. Besides, this work can reduce the required comparator path gains, the comparator power of this work is 6.1× smaller than [3] and 3.5× smaller than [4]. The reduced comparator power can significantly improve the power efficiency of the NS-SAR ADC, and makes the higher-order NS extension possible.

Table 1: Comparison of capacitor size and comparator power for the same kT/C and comparator noise budget

	C_{DAC}	C0	C1	C2	C_{total}	Comparator Gain Ratio	Comparator Power
Prior work [3]	C	C/3	C	C	10C/3	1:4:16	441×
Prior work [4]	C/5	-	3C/5	3C/5	7C/5	1:3:12	256×
This work	C/5	-	3C/20	3C/20	C/2	1:1.5:6	72.25×

Comparing to the works [5] and [6] which can also realize the passive gain, this work obviates the capacitor stacking and thereby reduces the signal attenuation on the integration signals, leading to better NS effect. Also, its integration capacitor size is 4× smaller than [5]. Besides, although the passive gain of this work is smaller than [6], the performance loss due to smaller gain can be compensated by using high-order NS.

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Fig.3 *Simulated spectrum.*

Simulation results: This work is verified by SPICE simulations. A 10-bit second-order NS-SAR ADC with NTF of $(1\text{-}0.75z^{-1})^2$ is designed. The simulated spectrum is shown in Fig. 3, it shows the second-order shaping noise slope. With the input signal frequency of 3.8 MHz and sampling rate of 200 MS/s, the SNDR is 83.2 dB in 20MHz bandwidth.

Conclusion: The work proposes a noise-shaping SAR ADC with 2× passive gain. Comparing to prior works, it can reduce the total capacitor size and comparator power consumption. It also obviates the capacitor stacking, leading to less signal attenuations. It has a simple circuit structure and is easy for high-order extension.

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